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THE MAGAZINE FOR QUALITY IN ELECTRONICS

Tim Teckman, engineering VP at MathStar.

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Test & MEASUREMENT WORLD®

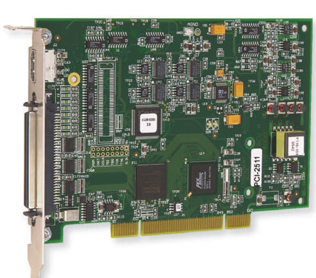
FEBRUARY 2007
VOL. 27 NO. 1

CONTENTS

FEATURES

Inspection / Page 35

DEPARTMENTS



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Guest commentaries

EDA *does* support Serdes test

Stephen Sunter of LogicVision disagrees with part of chief editor Rick Nelson's claims about ATE, BIST, and Serdes test.

IJTAG, SJTAG claims premature

Responding to a *T&MW* interview, CJ Clark of Intellitech says efforts to develop new IEEE JTAG standards are in the very early stages.

www.tmworld.com/guests

Sing along with Martin

"The Lab in the Corner," written and performed by senior technical editor Martin Rowe, tells the tale of a secluded, yet powerful, test engineer.

www.tmworld.com/labsong

Blog commentaries and links

Taking the Measure

Rick Nelson, Chief Editor

- One cheer, two jeers for job churn
- Vista's blue circle of death

Rowe's and Columns

Martin Rowe, Senior Technical Editor

- Get ready for pi day
- How smart should test equipment be?

Education and Careers

Amy Laskowski, Contributing Editor

- The ethical concerns of engineering weapons
- A laptop for every child

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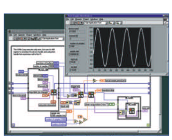

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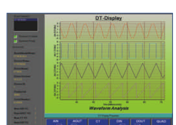

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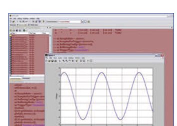

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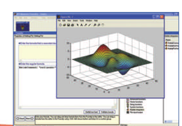

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Reed Electronics Group

Tree loses race with PC's CO_2

The climate is warming—that's a consensus reached by skeptics ranging from President Bush to Exxon Mobile executives. Bush in his State of the Union address cited "the serious challenge of global climate change," and an Exxon official told the *Wall Street Journal* that the company has softened its anti-global-warming stance because of improved climate models.

What to do about climate change remains contentious. Possibilities extend from worldwide implementation of the Kyoto Protocol (Bush and Exxon still oppose that) to individual carbon-reduction efforts. To support individual efforts, Dell is soliciting customer donations to help plant trees. A $6.31 tree, Dell says, will in 70 years absorb the CO_2 released by three years of PC operation.

RICK NELSON, CHIEF EDITOR

The problem with this plan is the PC's tremendous carbon-generation head start. Back-of-the-envelope calculations show that the PC will contribute 1.7 picodegrees Fahrenheit of global warming by the end of its three-year life; temperature rise will continue for 66 years, to 28 picodegrees, when the tree begins catching up.

The problem with Dell's tree program is the PC's huge head start.

Dell's program can make customers feel virtuous through a meager $6 donation tacked onto a PC purchase. But to truly offset a PC's carbon footprint, customers would need to donate about $140 to plant 22 trees for each PC purchased.

Then they would need to make sure their trees get planted in the tropics. Writing in the *New York Times*, Ken Caldeira, a scientist at the Carnegie Institution's department of global ecology, notes that trees in temperate climes absorb more sunlight than the farmland they replace, which offsets the cooling influence of their carbon sequestration. Trees planted in the tropics, however, help form clouds, which reflect energy back into space. (In response to one of my blog posts on this subject, Caldeira commented, "Dell is helping to preserve forests in the lower Mississippi valley, which would probably have some slight global cooling effect.")

All this is to say that climate change is too complex to be addressed at the individual level, even with a company like Dell handling the administrative work. Don't get me wrong—planting trees is good, and I hope Dell can generate significant donations to support reforestation. But keep in mind that Dell's effort is more of a marketing initiative than a serious effort to combat climate change.

What's truly required is what *Times* columnist Tom Friedman calls the "Green New Deal"—government programs and industrial projects to foster conservation and to perfect solar, wind, hydroelectric, nuclear, ethanol, biodiesel, and clean-coal technologies. T&MW

See the online version of this article for links to references and my climate-change calculation details: www.tmworld.com/2007_02.

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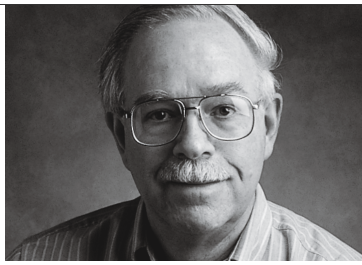

Into the bay: Buying a spectrum analyzer

In *Test & Measurement World*'s Test Voices column for November 2006, I offered some tips for shopping for used test instruments on eBay. To find out whether my advice was worth taking, I set out to purchase a used Hewlett-Packard spectrum analyzer. I compiled a list of general specifications, chief among which were frequency coverage to 1.5 GHz and an IEEE 488 interface. The instrument also needed to be in working condition and not a "fixer upper;" while spending bench time resurrecting dead equipment provides me with equal feelings of fulfillment and frustration, I have other projects to tackle.

After seeking well-informed opinions from RF and microwave engineers and technicians of my acquaintance, I settled on a Hewlett-Packard (now Agilent) HP 8568B. Although it's an obsolete instrument, Agilent provides service and operations manuals for the HP 8568B in Adobe Acrobat format on its Web site. Availability of documentation weighed heavily in my choice, as did availability of spectrum analyzers that offer backward-compatible programming code capabilities. I won't have to rewrite any code if I upgrade to a newer analyzer.

For a couple of weeks, I perused auction listings for HP 8568Bs in various states of condition. I settled on one offered by a test-equipment broker and described as "…fully tested, in working and excellent physical condition. Unit is very clean, with bright display screen and includes original cables and manual." I asked the seller a couple of questions regarding his packaging methods and received prompt and satisfactory answers.

Choosing the seller's "buy it now" option, I sent payment via PayPal and a week later, FedEx delivered two large cartons. Other work intervened, and a couple of days later I eagerly unpacked the cartons, connected cables to the analyzer's display and RF sections, and flipped the power switch. As the unit warmed up, I discovered in consternation that the RF section's front-panel logo read "8568A."

Had I been swindled? No, according to the seller. Someone in the warehouse had shipped the wrong unit, and he would send a replacement upon receipt of the 8568A. I immediately shipped the 8568A, and then the seller stopped responding to my e-mails and phone-call messages. A couple of anxiety-filled weeks elapsed before FedEx delivered the correct unit—an 8568B that looked cosmetically better than the first unit and operated flawlessly. Now, my real adventure begins: I'm looking forward to reacquainting myself with LabView while programming the 8568B to operate under IEEE 488 control. I'll keep you posted. T&MW

FOR MORE INFORMATION

To review my previous column and a few tips for purchasing instruments via an online auction, read "Test Voices" in the November 2006 issue:
www.tmworld.com/2006_11

When you're considering the purchase of an instrument via eBay, it's a good idea to ask the seller for the instrument's serial number, just in case you win the bid but receive another instrument with the same model number (and possibly different characteristics from the listed item). Auction sellers vary dramatically in their desire—or ability—to respond to a prospective bidder's inquiries. I didn't bid on two analyzers whose sellers didn't bother to reply to my questions.

Another buyer overbid me on an analyzer offered by a Canadian seller. Afterward, I read the seller's shipping instructions and noticed that the seller required the winning bidder's Social Security number. Apparently, in order for an item to get imported into the US, the purchaser must provide a taxpayer identification number or a Social Security number. Considering the potential for identity theft, I'm pleased that I didn't win the item in question. While legal documents make my eyeballs glaze over, I checked the following site, which includes the Social Security information in a subsection entitled "Import Requirements":
www.cbp.gov/linkhandler/cgov/toolbox/publications/trade/usimportrequirements.ctt/usimportrequirements.doc

You can view specifications for the HP 8568B at these Agilent sites:
cp.literature.agilent.com/litweb/pdf/5952-9394.pdf
www.home.agilent.com/agilent/product.jspx?nid=-536902968.0.00&cc=US&lc=eng

The HP 8568B's installation, operating, and service manuals are available here:
www.home.agilent.com/USeng/nav/-536902968.536881725/pd.html

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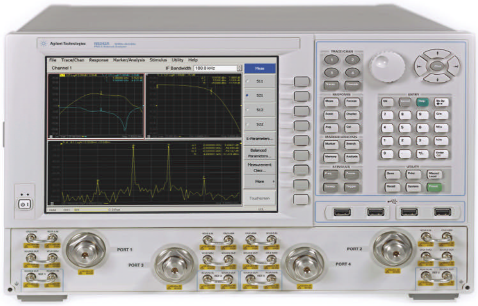


Agilent Technologies has introduced its 10-MHz to 26.5-GHz PNA-X microwave network analyzer, which features an integrated second source and signal-combining network. Configurable as a two- or four-port analyzer, the PNA-X employs a new signal-routing architecture that transforms it from a pure network analyzer to an RF measurement hub.

The PNA-X's feature set, said Agilent product marketing engineer Chad Gillease, enables engineers to make high-speed measurements on amplifiers and frequency converters without requiring complex multi-instrument setups. For example, he said, the analyzer's integrated second source can generate a fast fixed-IF or swept-LO signal for testing mixers, improving measurement speed up to 35 times, compared with using a traditional external source. In addition, he said, the PNA-X's internal pulse modulators and generators enable users to make pulsed-S-parameter measurements up to 30 times faster than would be possible with analyzers that require external generators and modulators.

Gillease described several specific applications, including a two-port two-tone amplifier intermodulation-distortion measurement, a four-port scalar mixer/converter measurement, and a four-port vector mixer/converter measurement.

Specification details at 24 GHz include +16-dBm power levels, –59-dBc harmonics, and 40-dB power-sweep range for the two internal signal sources. Dynamic range is better than 130 dB at 24 GHz, and the 0.1-dB receiver-compression value is 12 dBm at 20 GHz. Base price: $92,000. www.agilent.com.

VSO forms alliance with SDR Forum

The VITA Standards Organization (VSO) and the Software Defined Radio Forum (SDR Forum) have announced plans to collaborate on software-defined radio (SDR) specification activities underway at each organization. The initial focus of the relationship will be in the area of Digital Intermediate Frequency (DigitalIF) data transport. DigitalIF defines the signal and control data that is passed between the radio frequency (RF) subsystem and the baseband signal processing subsystem of an SDR.

VITA is developing the VITA 49 standard, which defines this data transport and allows manufacturers of these two types of subsystems to use a common data transport protocol, thereby simplifying integration and facilitating interoperability. The SDR Forum's System Interface Working Group (SIWG) is also looking at DigitalIF, with a goal of defining the requirements for a common set of application programming interfaces (APIs) that can later be standardized.

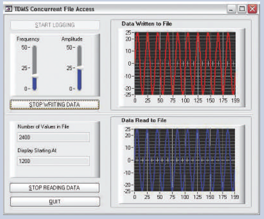
Collaboration between the SDR Forum and VITA ensures that the APIs will fully support the VITA 49 standard and provides a venue for VITA members to influence the API requirements. The SDR Forum is also examining the DigitalIF standards used by other industry associations operating in adjacent markets. This will ensure a robust API that fully addresses the needs of both VITA and SDR Forum members.

"VME technology played an early role in the development of software-defined radios," stated Ray Alderman, executive director of VITA. "VITA

Share data across networks

Editors' CHOICE

LabWindows/CVI, the C-based application-development package from National Instruments, adds the ability to share data over networks without TCP/IP programming. Version 8.1 adds a "network variable" that lets computers share data in the same way that global variables let code modules share data within an application. Thus, you can use a PC to monitor a test system over any network. The network variable is identical to the shared variable feature in LabView 8.0 and 8.2.



To make use of the network variable, a test-system controller PC must have an application written in LabWindows/CVI 8.1, and it needs the network variable engine installed. Remote-monitoring PCs need to use the LabWindows/CVI 8.1 run-time engine to gain access to the data in network variables. The version 8.1 run-time engine is backward compatible with applications written in previous versions of LabWindows/CVI, although applications written in previous versions don't support the new variable.

Base price: $1199. *National Instruments, www.ni.com/cvi.*

members quickly saw the need for a standard method to transport DigitalIF data over the various Gigabit-class data connections. The VITA 49 Working Group was established to address this need." SDRs are used in defense, public safety and security, and commercial applications such as RFID readers. www.vita.com; www.sdrforum.org.

Audio Precision opens accredited calibration lab

Audio Precision, maker of audio test equipment, has received accreditation from the American Association for Laboratory Accreditation (A2LA) for its calibration lab located in AP's Beaverton, OR, headquarters. All 2700 Series, ATS-2, and APx585 audio analyzers ordered from the company will now be calibrated before shipping.

Customers who purchased their audio analyzers before the new calibration procedure went into effect can send their equipment to Beaverton for calibration. Audio Precision will also calibrate any instrument sent in for valid warranty service within one year of purchase. www.ap.com.

CALENDAR

OFC/NFOEC, March 25–29, Los Angeles, CA. Sponsored by Optical Society of America, IEEE, and Telcordia. *www.ofcnfoec.org.*

SAE, April 16–19, Detroit, MI. Sponsored by Society of Automotive Engineers. *www.sae.org/congress.*

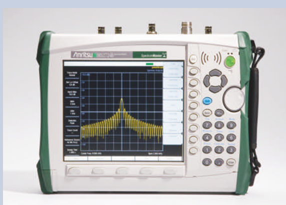
International Microwave Symposium, June 3–8, Honolulu, HI. Sponsored by IEEE Microwave Theory and Techniques Society (MTT-S). *www.ims2007.org/.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

Handheld spectrum analyzer reaches 20 GHz

Anritsu has expanded its Spectrum Master product line with the introduction of its MS2724B portable spectrum analyzer, which operates from 9 kHz to 20 GHz. In addition, the company has introduced its MS2721B and MS2723B versions, which offer frequency coverage up to 7.1 GHz and 13 GHz, respectively.



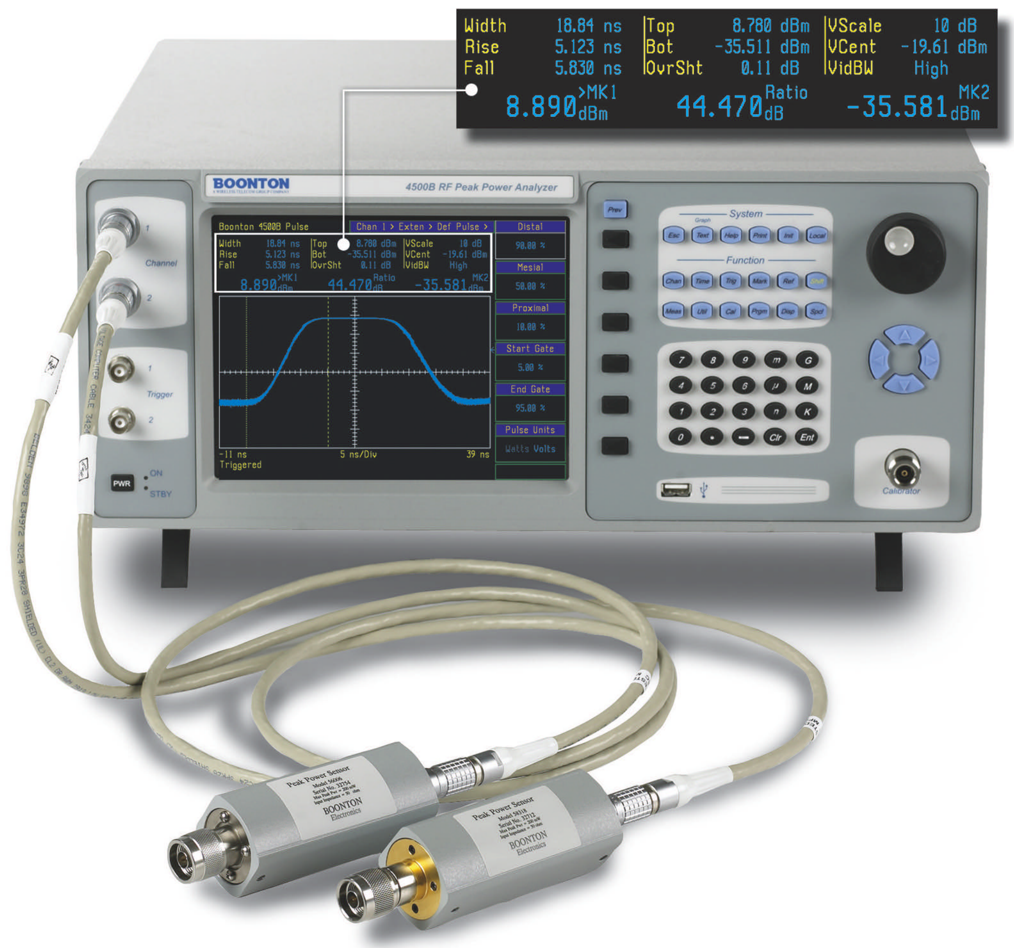
The MS2724B offers a low phase noise (typically –104 dBc/Hz at a 10-kHz offset from 2 GHz) and a 1-Hz to 3-MHz resolution bandwidth (RBW) range. The MS2721B has phase noise of –100 dBc/Hz at a 10-kHz offset up to 7.1 GHz, and the MS2723B has typical phase noise of –104 dBc/Hz at a 10-kHz offset at 2 GHz. The RBW range of these units is 1 Hz to 3 MHz, as well.

These three models are the first in the Spectrum Master family to feature a quasi-peak detector and CISPR-defined bandwidths for EMC precompliance testing. In addition, the MS2721B can be equipped with a tracking generator that provides calibrated output from 400 kHz to 7.1 GHz with a power range of 0 to –40 dBm in 0.1-dB steps. The MS2721B has typical displayed average noise ratio (DANL) of –163 dBm at 1 GHz in a 1-Hz bandwidth; the MS2723B and MS2724B deliver a DANL of –156 dBm at 1 GHz (1 Hz RBW) with the preamplifier on and –139 dBm with it off.

All three models also have a standard built-in AM/FM/SSB demodulator and built-in preamplifier. The instruments provide more than 2 hr of battery life.

Base prices: $13,950 to $20,950. *Anritsu, www.us.anritsu.com.*

We've Taken Performance To A New Peak.



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The buses roll on

PCI data-acquisition cards have been around for more than a decade. They handle a wide range of the measurement tasks, but PCI expansion slots are vanishing from commercial PCs. Those remaining slots are moving to the faster PCI Express serial bus. Thus, building measurement systems with PCI cards is getting harder to do.

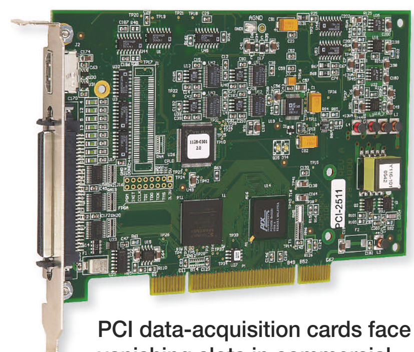
PCI also gets competition from PXI and USB, the latter of which is partly responsible for the loss of expansion slots. "USB is the hot bus right now," said Bill Kennedy, sales and marketing manager at Measurement Computing. Engineers are, however, building plenty of new systems with PCI cards.

In spite of the vanishing slots on PCs, PCI card makers report brisk sales. Industrial computers and expansion chassis help because they provide plenty of slots. Industrial computers also make it possible to use ISA cards, which card makers continue to build, although the rate has slowed significantly. Many ISA-based systems, though, require replacement cards, or engineers are asked to build duplicates of old systems.

Jon Tucker, lead marketing engineer for nanotechnology, research, and education at Keithley Instruments, said that card makers still build ISA cards because customers don't want to incur the costs associated with switching an ISA-based system to one that uses a different technology. "That's especially true with software," he added. Field wiring is another reason for not changing to a newer technology: A new card may use a different I/O connector that would be incompatible with the existing wiring.

Although engineers who need ISA cards can often still get them, card makers don't promote these cards anymore. "We still get orders for cards that use the ISA bus, the STD bus, and the Q bus," said Tim Ludy, product manager at Data Translation. "One person found an old card where the analog-to-digital converter (ADC) was a module instead of an IC and asked if we could build more boards with these modules. We'll make legacy boards for as long as we can get the parts."

"Customers pay a premium for ISA cards," added Kennedy. "We have to get parts made in through-hole packages, often from brokerage houses. If the part is available in a surface-mount package, then card makers may change their product to accommodate the newer parts, provided that there's enough sales volume to support an engineering change."



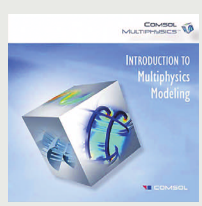
PCI data-acquisition cards face vanishing slots in commercial PCs. Courtesy of Measurement Computing.

Often, manufacturers of data-acquisition cards have to discontinue older products because IC makers discontinue their ADCs. When that happens, IC makers notify their customers (the card makers) to make a last-time buy. Card makers do the same for their customers to give them time to redesign their systems with newer technology.

Who uses PCI data-acquisition cards in new systems? All three people I spoke with mentioned machine builders who embed the cards into PCs to use as controllers. Other applications I've run across include test systems for automotive components where cost reigns supreme. Other applications include measuring systems where engineers don't want the measurement hardware accessible to operators. T&MW

For more on PCI and ISA cards, including past predictions, see my "Rowe's and Columns" blog at www.tmworld.com/blogs.

Free CDs on numerical modeling



COMSOL has released a series of free CDs that provide an introduction to numerical modeling. The CDs provide the basics of multiphysics modeling, acoustics simulations, RF simulations, AC/DC simulations (including electromagnetics), and reaction engineering. www.comsol.com/intro.

Instrumentation amp design guide

Analog Devices' *A Designer's Guide to Instrumentation Amplifiers* (3rd ed.) is now available, in both print and downloadable formats. The free book covers input coupling, specifications, matching instrumentation amps to ADCs, application problems and their solutions, and EMI reduction. www.analog.com/pr/freeinampguide.

Safety tester gets networked

Associated Research has added Ethernet communications to its Omnia line of safety testers. A card installed in the tester also adds local barcode capabilities for tracking test results to individual units. The 8100 series perform hipot, insulation resistance, and ground-bond tests. www.asresearch.com.


PUSH
TO TEST

STEVE SCHEIBER
CONTRIBUTING TECHNICAL EDITOR
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ICT faces the future

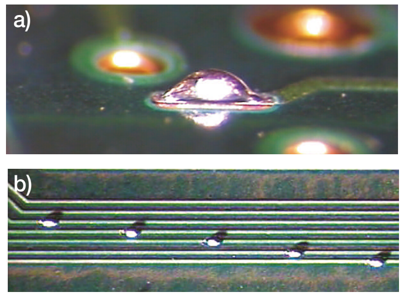
In-circuit test has defied its skeptics since the first analog test systems emerged more than three decades ago. The testers weren't fast enough. Digital logic would be their downfall. They couldn't find opens. They couldn't isolate circuitry sufficiently.

Today, little has changed. Test engineers must deal with denser circuits, eroding bed-of-nails access, higher speeds, and lower voltages, as well as the migration to lead-free solder. Yet, supporters of in-circuit test (ICT) have never wavered. Vendors have conquered each succeeding generation of PCB architecture. Alternatives such as functional test, boundary-scan, and system test have run into their own share of bottlenecks. ICT remains vital to most manufacturers' strategies for meeting quality targets.

Still, according to Chris Jacobsen, R&D manager for Agilent Technologies, ICT technology is at a crossroads. To survive as a weapon in the board-test arsenal, it will need to make a strategic shift more fundamental than "simple" design-for-testability. The current standard of specifying 35-mil test pads along a 5-mil board trace to accommodate the bed of nails consumes precious real estate and introduces additional fault sites. In addition, the pads are needed only until the board ships. But what choice do you have?

To find a solution, Agilent assembled the In-Circuit Test Measurement Science and New Technology Group, an in-house group consisting of Jacobsen and eight other engineers. Their less-than-obvious suggestion was to reverse the ICT roles of probe and target. Instead of hitting test pads on boards with sharp spring-loaded pins, the group recommended hitting sharp beads on the board surface with flat fixture pins.

Unlike test pads, bead nodes conform to the dimensions of the trace—about 5 mils wide and 15 mils long. The solder-deposition step places an oversized drop of solder on the board trace through an open-mask stencil.



**a) A bead node can make contact with a flat fixture probe during test.
b) No wider than board traces, bead nodes do not compromise circuit density.** Courtesy of Agilent Technologies.

During reflow, the wet solder flows along the trace, while its surface tension overcomes gravity, repeatedly creating a sharply pointed feature (**Figure 1a**).

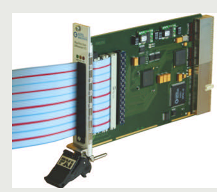
During testing, a flat 4-oz fixture probe makes contact with the solder bead. The bead's point begins to flatten into an ellipse until it can support the probe, in the process breaking up any bead contaminants that could interfere with the test. Jacobsen contends that the mechanical effect differs substantially from conventional sharp-pin node penetration. He likens the action to hitting a boiled potato with a frying pan. The potato's skin breaks up and falls away, exposing the inside.

Figure 1b shows one reason why design engineers will resist including bead nodes far less adamantly than their more traditional counterparts. Bead nodes do not require pushing board traces farther apart, so they don't compromise circuit density, and they don't affect the signal integrity of high-speed traces.

It appears that—once again—the report of the death of ICT has been greatly exaggerated. T&MW

PXI module for JTAG test of differential I/O

Goepel electronic's PXI-5350 3U single-slot module provides 50 bidirectional, differential channels, allowing for the test of differential connectors or backplanes. The test channels are individually programmable as input or output and allow simultaneous driving and measuring. In contrast to conventional boundary-scan I/O modules, the PXI-5350 is not controlled serially through a test access port (TAP) but through a parallel PXI interface to increase test-vector throughput. www.goepel.com



iNEMI to preview roadmap at Apex

The International Electronics Manufacturing Initiative (iNEMI), an industry-led consortium, will preview its 2007 roadmap at this year's IPC Printed Circuits Expo, APEX, and Designers Summit in Los Angeles. The roadmap will be featured in a keynote session at 8:00 a.m. on Thursday, February 22. The 2007 roadmap will be formally released after March 5, but this keynote session will provide a "sneak peek" at some of the highlights and trends identified by the roadmap. www.inemi.org.

IPC Midwest Conference & Exhibition gains support

In the month following the December 13 announcement of the new IPC Midwest Conference & Exhibition, test-equipment maker SPEA America has joined six other companies in announcing their commitment to exhibit. The event, targeted at the electronics assembly and PCB manufacturing industries, will take place September 23–28, 2007, in Schaumburg, IL. www.ipc.org.

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Agilent Technologies

DIGITAL VIDEO TEST

Three-step test verifies video equipment

MT VERNON, NY—Key Digital Systems manufactures audio and video distribution amplifiers and cables. Often found in sports pubs, hotels, and in some homes, the amplifiers take in analog or digital video from DVD players and set-top boxes and distribute it to TVs in either digital high-definition multimedia interface (HDMI) format or analog format.

Key Digital has reduced design-verification testing to just three steps (**figure**). The lab houses racks of set-top boxes and DVD players and has TVs from numerous manufacturers.

Tests start with the physical-layer (PHY), where systems and hardware design engineer Yury Wolf-Sonkin checks eye diagrams on the HDMI streams for compliance to standards. He uses a 6-GHz real-time oscilloscope with built-in HDMI-compliance software to analyze the eyes. "PHY testing comes down to eye openings," said Wolf-Sonkin. "The eye must have at least a 38% opening at the receiver."

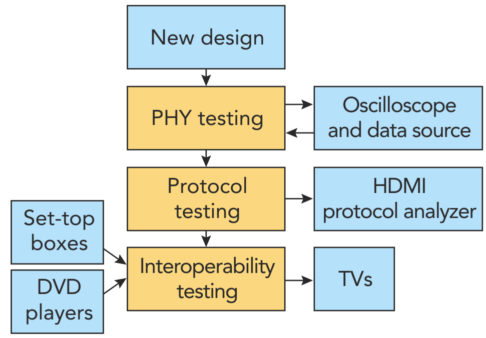
The remaining tests revolve around software. Wolf-Sonkin uses an HDMI protocol analyzer to verify that a distribution amplifier's transmitted video and audio streams meet specifications. It also checks video sources for HDMI implementation.

Because a distribution amplifier must connect to both a video source and to a TV, interoperability testing requires connecting a distribution amplifier to a wide array of products that lets Key Digital engineers find problems so users won't.

"The HDMI standard leaves some things open to interpretation," said Wolf-Sonkin. Thus, an HDMI stream may not be compatible with every TV. Interoperability testing lets Key Digital engineers verify that a distribution amplifier's software can handle these issues.

For links to sources of technical information about HDMI, see the online version of this article at www.tmworld.com/2007_02.

Martin Rowe, Senior Technical Editor



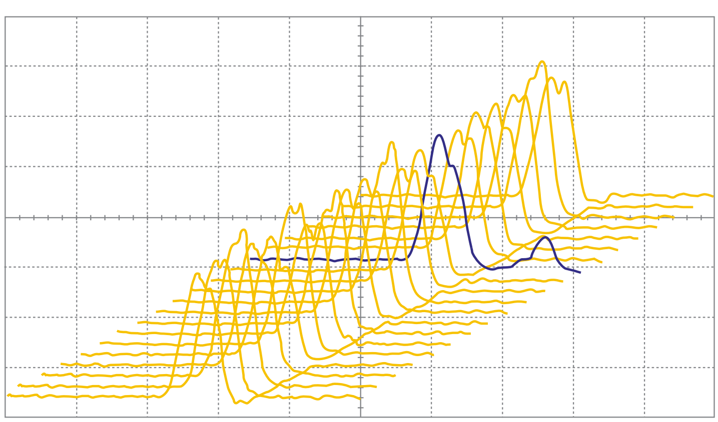
Engineering tests of video distribution amplifiers consist of physical-layer tests, protocol tests, and interoperability tests.

WEBCAST

Oscilloscopes track intermittent signals

The oscilloscope is one of the most familiar test-engineering tools—one whose operation you mastered in college, if not sooner. But scopes continue to evolve, and that one on your bench may offer valuable capabilities of which you are unaware. In the Webcast "Finding and Troubleshooting Intermittent Signal Faults," Dr. Michael Lauterbach, director of product management for LeCroy, describes a variety of functions that you can use to isolate runts, glitches, and other signal abnormalities.

Lauterbach begins by describing persistence mode, which color-codes waveforms based on how often they occur—for example, the most common signal shape appears in red, with the less common shapes spread through the spectrum toward violet. He notes how a persistence mode can help you identify anomalies such as an infrequently occurring after-pulse, and he explains how you can use a waterfall display generated by a sequence mode to help obtain more information about such an anomaly—for instance, that an after-pulse occurs once every 20 traces (**figure**). He also introduces a replay



A waterfall diagram generated in sequence mode can help you determine how often an after-pulse anomaly (shown in blue) occurs.

Oscilloscopes track intermittent signals *(continued)*

mode, which lets you investigate waveform history to help track down runts and glitches.

Scopes are primarily time-domain tools, but most can provide statistical-domain views as well, which Lauterbach says can provide the best way to characterize the amount of instability in a key signal parameter. He notes that you can use a histogram display to see the maximum range of parameter values, their RMS variation, and the shape of the distribution.

The Webcast also covers exclusion triggering, which provides a way to trigger on a rare signal fault when you do not know what the fault looks like. With an exclusion trigger, you might, for instance, ask your scope to trigger upon encountering clock pulses that are less than 980 ns or greater than 1.02 µs. Lauterbach discusses the use of an exclusion trigger in combination with persistence mode—a technique that can help you find signals with rise times that are too fast (and therefore could cause crosstalk) or too slow (and therefore could cause timing problems).

Lauterbach also describes eye diagrams and mask testing, and he explains how you can determine whether a failure is coincident with crosstalk, with power-supply noise, or with some other trouble source. He concludes by describing a waveform-search function that can help you locate and analyze rare events that can't be captured using hardware triggering schemes.

You can view the archived Webcast, sponsored by LeCroy and *Test & Measurement World,* at www.tmworld.com/webcasts.

Rick Nelson, Chief Editor

NETWORKING EQUIPMENT

Networking equipment may need more test

"37% of IT and 46% of home users of networking equipment reported experiencing problems with the functionality of networking equipment purchased in the past two years." That's one of the findings of a survey conducted by King Research in October 2006 for the Fanfare Group, a maker of test-automation software.

The survey (Ref. 1) concludes that networking equipment such as DSL modems and wireless print servers are still hard to set up. "What surprised us," said Fanfare marketing manager David Gehringer in a phone interview, "was that such a large percentage of IT users reported problems. We expected a high percentage of home users to have problems, but we assumed that IT people, who have experience with networking equipment, would have an easier time."

According to Gehringer, most calls to technical support resulted from poor user interfaces and poor documentation. But Gehringer pointed out that IT people also report dropped packets or improper forwarding and routing. Still, users are resilient, with less than 5% of the respondents saying that they returned products to vendors without calling technical support. Before people call for technical support, they often look online, with Google being the first place they go.

Interoperability may also be an issue, especially when people connect new equipment to old computers or other networking products. Manufacturers can't test their equipment under every possible installation. They may also be reluctant to produce in-depth user manuals because of printing costs. Instead, they rely on short manuals and quick-start guides, which may cover a significant portion of users but will leave others wanting more information.

Martin Rowe, Senior Technical Editor

REFERENCE

1. "Survey of Networking Equipment Quality," King Research, November 2006. A link to the survey is available in the online version of this article at www.tmworld.com/2007_02.

RF TEST

The analog in software radio

DEVICE UNDER TEST
SDR modules that mount onto VMEbus single-board computers. The modules contain ADCs, DACs, digital upconverters and downconverters, timing logic, memory, a PCI interface, and an FPGA.

THE CHALLENGE
Test the performance of the analog and digital portions of the SDR. Test ADCs and DACs for dynamic range, signal-to-noise ratio, linearity, and intermodulation distortion. Test digital upconverters and downconverters, timing logic, and memory.

THE TOOLS
- Agilent Technologies: spectrum analyzer, signal generator. www.tm.agilent.com.
- Meterman: handheld DMM. www.metermantesttools.com.
- Pentek: single-board computer. www.pentek.com.
- RLC Electronics: bandpass filter. www.rlcelectronics.com.
- SBS Technologies (now GE Fanuc Embedded): VME-to-PCI bus adapter. www.gefanucembedded.com.
- Tektronix: oscilloscope. www.tektronix.com.
- Wenzel: 100-MHz oscillator. www.wenzel.com.

PROJECT DESCRIPTION

A software-defined radio (SDR) is a wireless communications system that digitizes modulated signals as close to the antenna as possible. An SDR processes signals using digital algorithms instead of analog circuits. Pentek (Upper Saddle River, NJ; www.pentek.com) produces an SDR dual-channel transceiver.

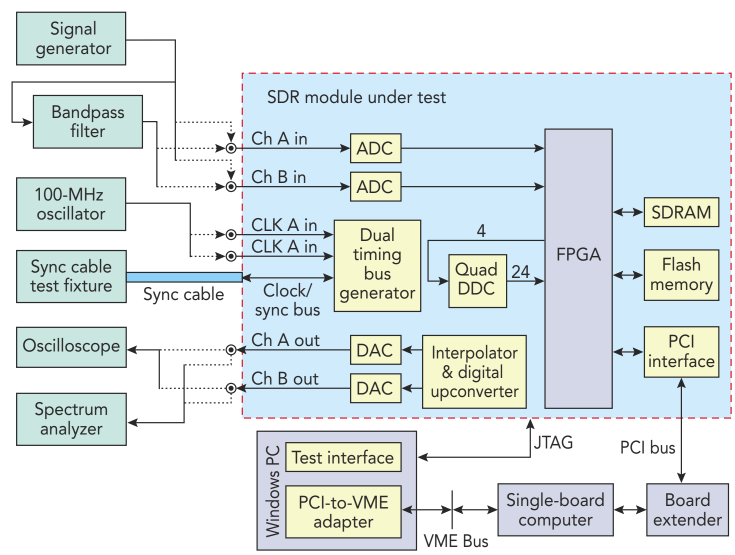
Each SDR module contains two analog-to-digital converters (ADCs) and two digital-to-analog converters (DACs), one pair for each channel (**figure**). Because the digital portion of the SDR is in software, the analog portion of the card requires the most testing. Pentek measures many of the characteristics that ADC and DAC manufacturers measure: spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), linearity, and intermodulation distortion (IMD).

The SDR module attaches to a VMEbus single-board computer (SBC), which attaches to a PC through an adapter. After applying power to the unit under test (UUT), a technician measures voltage with a digital multimeter (DMM). Automated testing begins with a boundary-scan test. Then, the technician moves to analog testing.

The ADC tests include an input-overload-detection test to verify the SDR's full-scale accuracy and overload signal detection levels. Technicians also perform an ADC channel-synchronization test and a decimation test, which lets them check the programmable decimation stage that follows the ADCs. These tests check both channels using 10-MHz outputs from the signal generator.

To measure the signal quality of the ADCs, a technician inserts a 70-MHz bandpass filter in series with the signal generator to remove unwanted harmonics and spurious signals from the generator's 70-MHz output signal. The technician measures the SNR, SFDR, and IMD of the ADCs. The test of the digital downconverter (DDC) uses ADC data to drive the DDC's input. Output data from the DDC goes to the FPGA, PCI interface, and SBC and then to the PC for analysis.

In a DAC test, the SBC sends a digital baseband signal into the UUT, which sends it through the DAC to both analog outputs. The technicians use an oscilloscope to view the DAC analog outputs in the time domain, and they use a spectrum analyzer to see the outputs in the frequency domain. Technicians also perform digital tests. The external clock test verifies that both external clock inputs are functional and that the operator can switch between internal and external clocks.



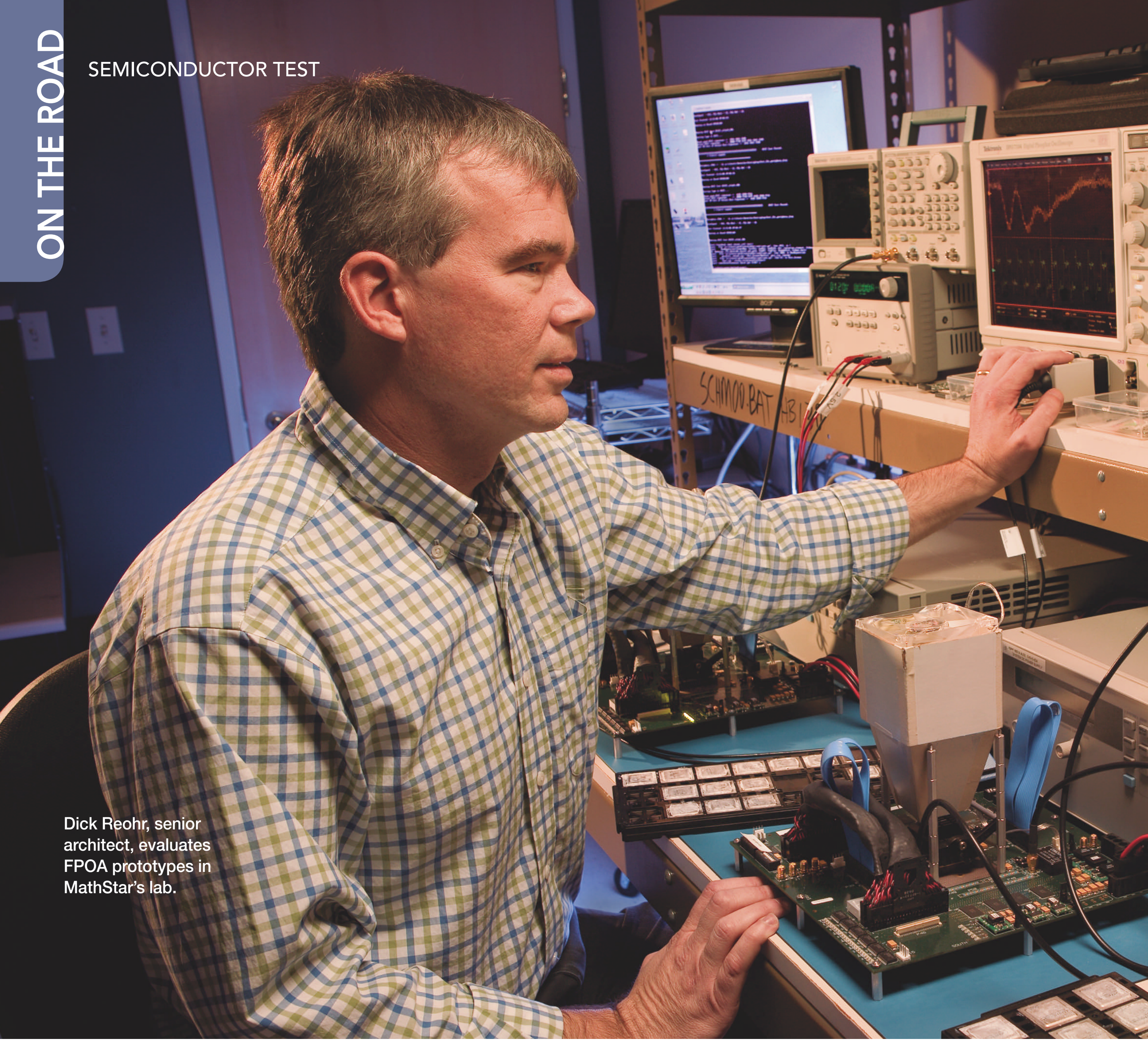
SDR modules require rigorous testing of their ADC and DAC analog circuits.

LESSONS LEARNED

"Boundary scan is essential for troubleshooting and testing the many high-density BGA devices on a board," said Pentek VP Rodger Hosking. "Maintaining adequate analog signal integrity in the midst of digital circuitry is also essential." Hosking noted that good signal integrity requires clever board layout strategies plus careful assembly, inspection, and testing.

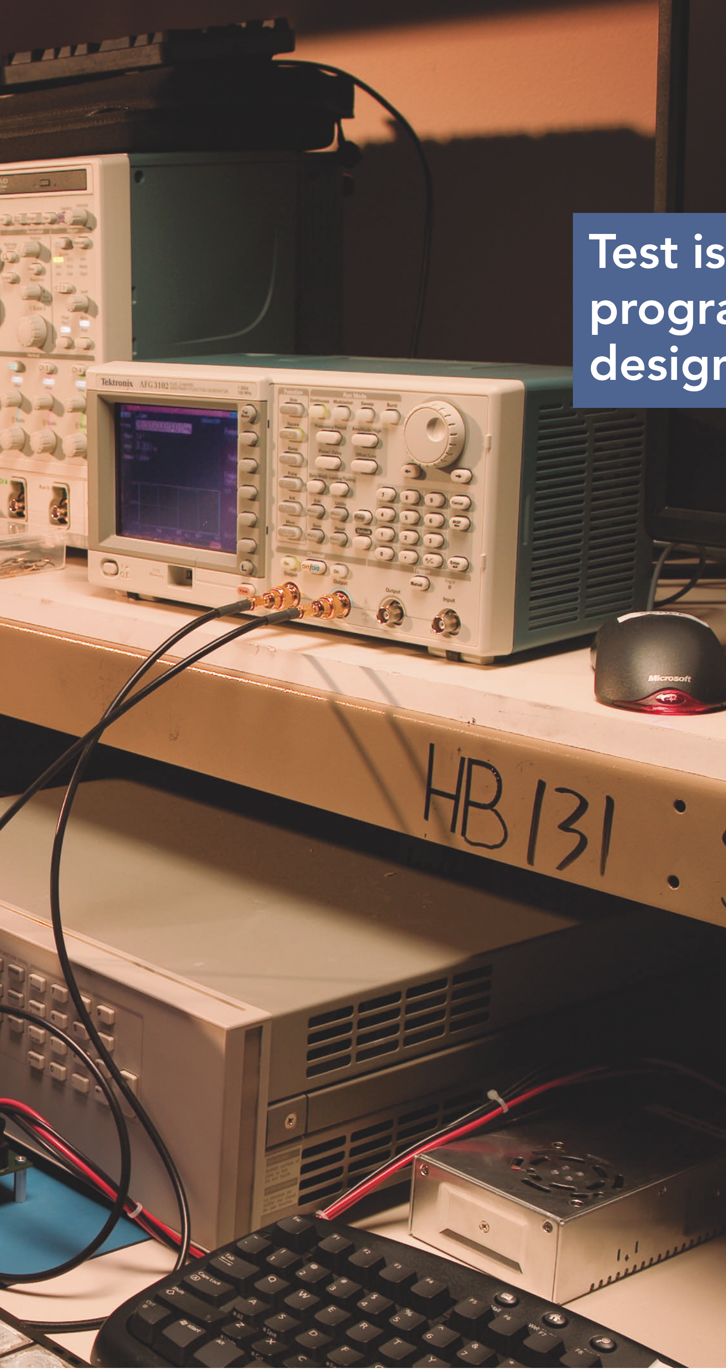
Martin Rowe, Senior Technical Editor

SEMICONDUCTOR TEST



Dick Reohr, senior architect, evaluates FPOA prototypes in MathStar's lab.

Computational VISION



PETE STONE/NPN WORLDWIDE

Test is a key part of moving field-programmable object arrays from design into manufacturing.

RICK NELSON, CHIEF EDITOR

HILLSBORO, OR—Traditional approaches for extracting computational power from silicon are insufficient for meeting the requirements of machine-vision, professional-video, medical-imaging, radar-processing, and other demanding applications. That's the view of the founders of MathStar, who envisioned a silicon computational device that could provide the performance of ASICs at the development costs of FPGAs. The device they invented is the field-programmable object array (FPOA)—a high-performance, reprogrammable integrated circuit based on the company's proprietary silicon object technology, which in its second-generation Arrix family of devices can process logic functions at a clock rate up to 1 GHz.

Underlying the FPOA's development was the Minneapolis-based founders' extensive knowledge of how to efficiently implement in silicon the massively parallel processing required to quickly execute the complex algorithms required in machine-vision and other demanding applications. MathStar founder and president Douglas Pihl said the concept arose when he was working with a mathematician on DARPA-funded projects related to making supercomputing platforms sufficiently fast to serve in very high-performance computing radar detectors. "It made sense," said Pihl, "to start a company that would build chips to serve these applications."

"We didn't believe that FPGAs were going to be able to keep up with the performance demands. We originally thought we would build ASICs. But we saw that ASIC development costs were at half a million dollars and rising, and we didn't believe the algorithms we planned to implement would serve enough market segments to make an ASIC implementation profitable."

Pihl said he did believe, though, that "the market would be receptive to a product that filled the gap between FPGAs and ASICs—one embodying a programmable architecture coupled with gigahertz-rate performance. A lot of people were saying they couldn't afford to spend a half million dollars to make an ASIC. A lot of people have adopted FPGAs, which have been very useful, but we saw that technology plateauing. People were finding that their application would require two or three or four FPGAs—and that's just too bulky and cumbersome. So, we thought the market would be very receptive to a new technology."

He added, "We also felt our new device had to be programmable, or we would have the same development cost problem facing ASICs. We worked a long time on developing an architecture thoroughly focused on performance and programmability—maintaining our goal of getting it to run at a gigahertz and still be a very programmable architecture."

Unlike FPGAs, FPOAs are not user-programmable at the gate level but rather at a higher, silicon object level. Object types now include arithmetic logic units (ALUs), register files (RFs), and multiply/accumulate units (MACs), each of which is programmable (**Figure 1a**). The objects themselves are arranged in an internal grid pattern, surrounded by functions such as memory and I/O. The object grid is overlaid with a patented, high-speed intercon-

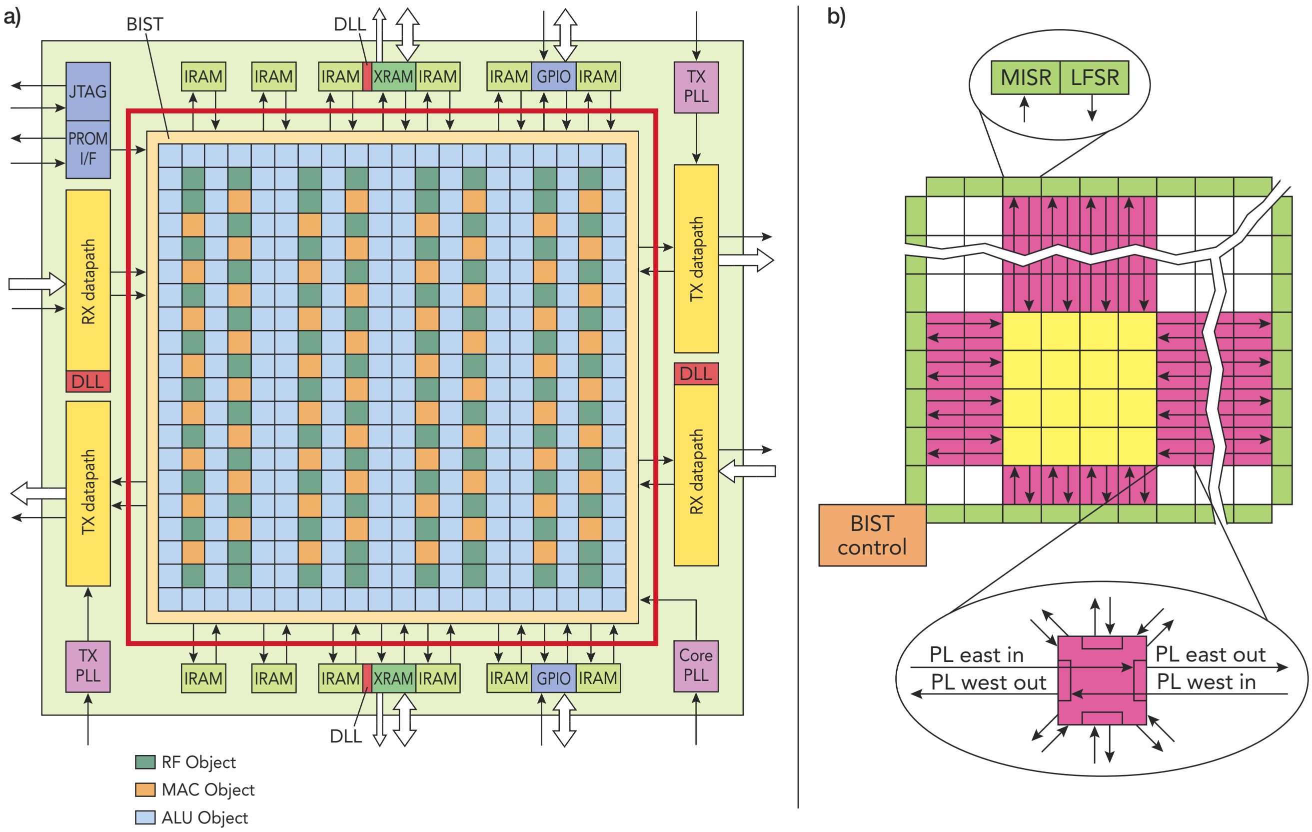


FIGURE 1. a) In an FPOA, a periphery surrounds a core consisting of arithmetic logic units, multiply/accumulators, and register files. The core (inside the red line) operates at 1-GHz and requires BIST; other components operate at slower speeds and are amenable to ATPG techniques. b) MISRs and LFSRs communicate with objects in a rectangle under test over party lines.

nect system that a customer programs to serve unique applications.

Rad-hard advantages

The FPOA architecture has benefits in addition to performance. Explained Pihl, "Some of our very early customers were in the mil/aerospace area and were always looking for highest performance. Several years ago, we started talking with Honeywell's space electronics group. They had looked very seriously at FPGAs, but they wanted to make them rad hard. Because of massive amounts of SRAM in an FPGA, that's very difficult. They would have had to use triple-mode redundancy to get around the soft-failure problem. Because of the space and weight and power-supply limitations, it just wasn't practical. Our device is much more attractive in this respect because it has only 10 to 15% of the SRAM in FPGAs. Ultimately, we expect them to port our device over to their rad-hard facility in Minneapolis."

Engineering VP Tim Teckman noted that FPOAs require less SRAM because the hard-wired silicon objects don't require gate-level programmability. "Because the functions that we deliver in objects are higher-level functions, there are fewer programmable states. An ALU, for example, has 30-some instructions and a number of states that we can program with a few hundred bits. If you are going to build an ALU out of CLBs and LUTs, you are going to have literally thousands or maybe millions of bits of configuration information. Because we have already done the detailed design and optimization, the end user doesn't have to program those functions."

Added Pihl, "The same applies to the interconnect structure. With an FPGA, you are making connections all over an array, and each path includes a whole bunch of pass transistors, each of which takes a configuration bit. With our chips, you need just a few bits to specify the destination and operation, and off it goes. Also, we use the same basic PROM-loader or JTAG-loader mechanism as do FPGAs, but since we have fewer configuration bits, configuration time is much shorter."

You might expect that deep-pocketed military and aerospace prime contractors would opt for rad-hard ASICs, but Pihl explained that even for the government, ASICs are becoming too expensive. And a bigger problem, said Pihl, is that invariably a development team will get halfway through an ASIC design, and system designers and mathematicians will say, "wait, we improved the algorithm—do it this way," resulting in huge cost and schedule delays. "They want programmable solutions," said Pihl. "They even talk about reprogramming satellites in space."

MathStar developed its original technology in Minneapolis and maintains a design team there. But Pihl believed that to grow the company and move the product from prototype to production, it would be necessary to move to

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an area offering a wealth of semiconductor talent. "A lot of ASIC designers know how to work with standard libraries, but finding people that really understood silicon—especially at the transistor level—was tough. After we got through the initial development and produced our prototype chip, I felt that if this was really going to work, we had to move to a different area. It's one thing to build a prototype chip that works, but quite another to make a million."

So in early 2005, the company established its Hillsboro, OR, headquarters and brought onboard, among others, engineering VP Teckman, COO Dan Sweeney, and marketing VP Sean Riley, all of whom had worked at Intel. Teckman's job was to reorganize the engineering team to be more process oriented with a much heavier emphasis on test and simulation and timing extraction. Having shipped its first prototypes in April 2005, the company in July 2006 received its first 1-GHz production units from foundry TSMC.

Teckman said that the parts that went into production in the fourth quarter of 2006 are 130 nm. Added Pihl, "When we started, 90 nm was very early edge. We heard horror stories, and we said we didn't want to take the process risk along with the architecture risk. Now, with Tim, we have more process knowledge, but we still we feel we can get the performance through the architecture, so we can afford to hang back a process step or so."

Added Teckman, "We are doing some interesting things with the process to maximize the performance we get out of it. We've started work in the 90-nm process space, but we prefer to stay off the bleeding edge of process technology as a smaller company, because we are able to hold back and still have 2X or so clock-rate performance improvement.

"That said, we don't think our technology is in any way tied to any particular process. We can use the same sort of architecture and design techniques on the processes as they mature. But there is a huge cost in terms of time and resources and dollars associated with being on the leading edge, and we don't think we need to be there. We are delivering the performance without it."

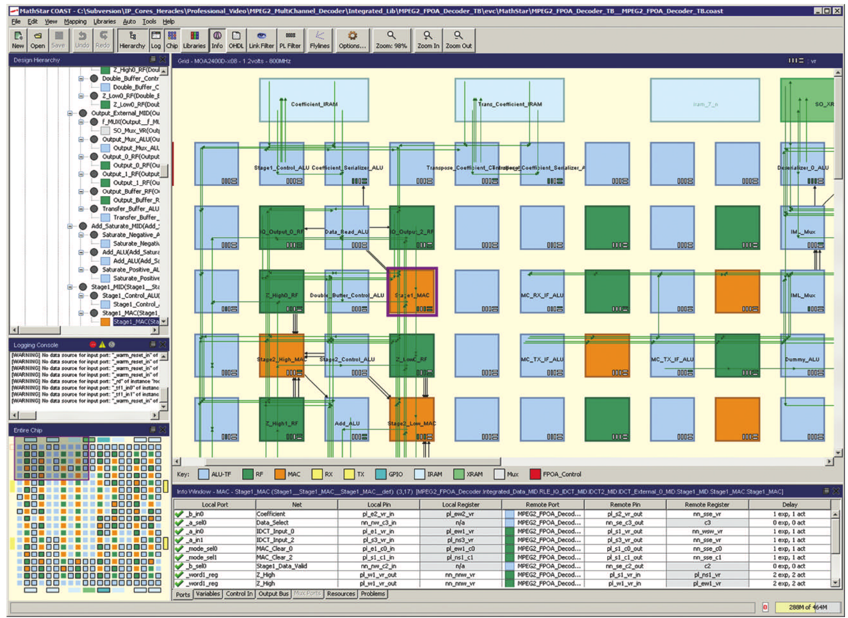

FIGURE 2. Users can convert a logic design into a physical FPOA implementation using MathStar's COAST tool, which provides a graphical user interface for placement and connection of the silicon objects. Courtesy of MathStar.

BIST supports gigahertz performance

The FPOAs' built-in self-test (BIST) implementation helps MathStar maximize performance while providing 98% fault coverage for both stuck-at and speed-related faults, according to Dick Reohr, senior architect. He described the FPOA structure as a prelude to explaining how test works: "The object array is a matrix of symmetrical objects that connect together by abutment, so we can easily change the size and shape and tiling pattern of the array, which operates in synch with a common 1-GHz clock. Surrounding the array is a ring of circuitry we use for BIST."

That circuitry (**Figure 1b,** top inset) consists primarily of linear-feedback shift-register (LFSR) pseudorandom number generators, which provide stimulus traffic into the object array, and multiple-input shift registers (MISRs), which record and compress results.

"Outside that collar," Reohr continued, referring to the red square in Figure 1a, "are periphery interfaces that operate with many independent and substantially lower-speed clocks. For example, the external memory operates at 175- to 266-MHz DDR, the parallel LVDS at up to 500-MHz DDR, and the GPIO at 100 MHz. The RTL code describing the periphery interfaces is all written in Verilog, and we use a scan ATPG methodology to test the periphery devices."

(continued)

Table 1. High-level BIST algorithm

Step	Procedure
1.	Disable I/O.
2.	Shift in rectangle under test (RUT) infrastructure into entire array with RUT at bottom left.
3.	Shift in random seeds to LFSRs; initialize MISRs and signature register.
4.	Enable full-speed clocks for burst of activity; provide random stimulus and record outputs to MISRs.
5.	Shift LFSR chains to reconfigure objects under test.
6.	Repeat steps 4 and 5 a configurable number of times.
7.	Record state of MISRs into final BIST signature.
8.	Shift all objects one column to the right. RUT moves east one column.
9.	Repeat steps 4 through 8 a configurable number of times.
10.	Repeat steps 2 through 9, moving RUT up one row, a configurable number of times.
11.	Read and compare final BIST signature.

Within the collar, Reohr continued, "test is a little bit tougher. We faced a tradeoff between performance and adding testability hooks, and because of the delays scan muxes would impose, we chose not to add scan. So, we needed to come up with some other way to test the internal array. We had to come up with a BIST algorithm that was scalable—that would allow us to change the shape of the object array as well as the tiling pattern. Each object is unique, but from a BIST point of view it must be self-testable using the same BIST algorithm—that is, the BIST algorithm must be independent of the tiling pattern. We also need to run tests at the full gigahertz clock rate, so we had to disassociate ourselves from any particular tester—we shift test data in and out at slow speeds, turn BIST on, and let the chip manage all the high-speed signals itself."

One of the biggest challenges, Reohr said, stemmed from the fact that BIST "configures the part in a random way that's not realistic"—that is, that doesn't mirror how the device will run during normal operation—"and the amount of power that we could potentially consume could be too great, so we had to make sure we limited test power to levels that would permit wafer tests without requiring cooling. Another challenge involved the fact that random configurations established by the BIST circuitry could conceivably require a signal to traverse the full array in a single clock cycle, whereas single-clock data transfers by design occur only within local neighborhoods."

Reohr employed the concept of a "rectangle under test" to address these challenges. In Figure 1b, the yellow objects represent the rectangle under test, and they are fully powered up. The white objects are powered off to limit chip power consumption, while the red objects are partially powered up to allow the party-line (PL) buses that connect all objects together to carry data into and out of the rectangle under test. The lower inset in Figure 1b details an object's east/west PL bus.

MathStar founder and president Douglas Pihl said MathStar moved its headquarters to Hillsboro, OR, to tap the area's wealth of semiconductor production talent. Courtesy of MathStar.

The rectangle under test, Reohr said, can range from 1x1 to nx8, with the exact configuration downloadable via the JTAG interface. Large rectangles help to verify timing over varying multicycle paths, but they reduce observability. Test typically begins, he said, with the rectangle in the lower left. The rectangle is then marched from left to right and then moved up one row, with the process repeating until test is complete. **Table 1** outlines the BIST algorithm.

Test and simulation

Device test is only part of the challenge of getting customers' products up and running. MathStar also needs to support its customers' efforts to develop and test FPOA applications.

To that end, Teckman said, the company offers a variety of applications support. "We have several types of development kits that provide a chip and programming tools and some applications libraries along with training. We offer one development board that connects to a PC, and for military/aerospace applications, we provide a ruggedized rack of DIN cards that includes a control processor and an FPOA. We have an internal IP development team that builds things like FIR filters and FFTs for the test-and-measurement applications—for front-ending an oscilloscope probe, for instance. In addition, third-party IP developers like Barco Silex and Cadre Codesign, which have made a business of building IP on top of FPGAs, have now started to migrate to our technology."

Steve Kassel, director of silicon/system engineering, explained the application

development process. "Tool flow starts with Summit Design's Visual Elite—that's our design entry tool, which we use to generate OHDL, or Object Hardware Description Language, a Verilog-like syntax we use to pass information between our various design tools. Customers then use COAST," MathStar's Connection and Assignment Tool (**Figure 2**), "for floor-planning and placement. When the layout is complete, a compiler combines OHDL and mapping files to generate the image that's downloaded onto the target chip."

Teckman said that customers can't rearrange the silicon objects for chips they already have—they can only reprogram the connections. He explained, however, that an Excel spreadsheet and a Perl script are all that are necessary for specifying a custom array that MathStar can build. "We do that for our internal development, and Barco Silex and end customers all get access to this capability." Ultimately, he said, the goal is to take a simulation in a program like Matlab from The MathWorks and synthesize directly to objects, with automatic place-and-route.

As an example, said Teckman, "We are doing something like that today with Barco Silex, which has built a complementary FPGA that sits next to an FPOA. Barco Silex uses our tool with Visual Elite from Summit and ModelSim from Mentor Graphics to form an environment where they simulate a complete design."

Teckman emphasized that throughout the design process, the customer is not dealing with clocks or DLLs (delay-locked loops) that could affect timing closure. Data transfer timing between nearest neighbors or over party lines is completely deterministic, with nearest neighbors and all party lines synchronized to the exact same clock.

Said Pihl, "An advantage of our architecture and our tools is that we have deterministic timing. We can load a program, and it runs at the full 1-GHz clock rate. You won't have the clock-rate degradation as in FPGAs, which have a place-and-route and timing-closure iterative loop you have to go through. With FPOAs you can literally simulate the timing and performance of your application, because we have cycle-accurate models of each one of the objects in our chip. A customer can know exactly what his timing is before implementing real hardware, making for a very efficient design process."

Pihl added, "We want to evolve the toolset over time to make them easier to use. Our current tools are based around Summit Design's Visual Elite, and we are trying to expand that to deal with a whole range of EDA companies, so customers can use the front-end design tools they already have." The goal is full support for ESL, he said. "We want customers to have the ability to do SystemC level simulations and move down the hierarchy toward automated development of the actual code that runs on our chips." T&MW

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AOI systems SIMULATE HUMAN BRAIN

PAMELA R. LIPSON, IMAGEN AND LANDREX TECHNOLOGIES

Every day, on countless assembly lines, humans serve as quality inspectors. Their supervisors "program" them by showing them good samples and by describing some faults to watch out for. By extrapolating the information, the human inspectors can flag various kinds of problems without having been shown exact examples beforehand.

In terms of ease of programming, humans are hard to beat, but we do have downsides. Humans are expensive and are too slow to keep up with the frenetic beat rates of today's assembly lines. Our eyes are not good enough to match the output of ultra-fine manufacturing processes, and we have difficulty keeping focused on very repetitive tasks. As a result, human inspectors are giving way to automated optical inspection (AOI) systems.

Of course, current AOI systems also have limitations. They are quite brittle to acceptable changes in the appearance of the boards, parts, paste, and solder joints, and the process of programming the systems can be time-consuming and expensive. Some AOI systems need constant modification to accommodate acceptable variations in the appearance of a printed-circuit board (PCB) and its components. Without constant "tweaking," an inspection program that currently exhibits low false failures and low false accepts may change its performance adversely over time.

What can be done to make AOI systems easier to program and maintain? The answer may lie in the human brain.

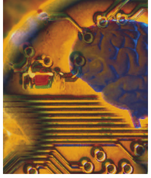
Applying brain science to AOI

Advances in brain science over the past 15 years have been dramatic, partially because inventions such as magnetic resonance imaging (MRI) machines have made it possible to see the brain in action. Researchers have learned several lessons that can be directly applied to improving the intelligence of PCB AOI systems.

Naturally, some people may justifiably be skeptical. For instance, exaggerated claims of being able to create HAL from the Stanley Kubrik movie *2001: A Space Odyssey* by the year 2001 led to great disappointment. Also, researchers who wanted to model the neuron and incorporate silicon neurons (popularly known as "neural networks") in optical inspection machines have managed to achieve only marginal performance.

But with recent advances in brain science, researchers have learned more about the functionality of the human brain and have been able to implement their findings in artificial intelligence systems. There are five principles integral to brain function that can be employed in AOI systems to make them more reliable and resilient to changes as well as easier to program and maintain.

By mimicking the adaptability of the human brain, manufacturers are building inspection systems that exhibit a high level of performance over extended periods.



Principle 1: Collective action

Brains are inherently modular, with sensory information being sent in parallel to multiple areas of the cerebral cortex. These areas analyze the inputs in different ways, and their results are pooled (Ref. 1). This style of functioning is akin to a community in which each member has his or her own domain of expertise (Ref. 2). Each member's performance might not be sufficient alone, but their collective action confers tremendous advantages to the whole assembly.

In the domain of machine learning, this idea has come to be known as "boosting," or combining multiple, possibly weak, classifiers to produce one that is surprisingly powerful (Ref. 3). Using this approach when building a machine simplifies the design (since it dispenses with the need to create one monolithic system), and it allows the system to be more adaptive.

In the case of an AOI system, each member of the community would correspond to a software agent that specializes in a particular kind of inspection (**Figure 1**). For instance, one agent might look for the appearance of the object under test, another might look at its edges or transitions with the board, and a third might look for the board that is supposed to be underneath the part.

Agents that are confident participate in the pass/fail decision, whereas the opinions of less-confident agents are either weighted less or dropped out of the decision. Such a system is more fault tolerant than a monolithic one due to the built-in redundancy, and it is also easier to modify. Engineers can replace or remove agents without drastically modifying the system architecture in order to adapt to changing inspection criteria.

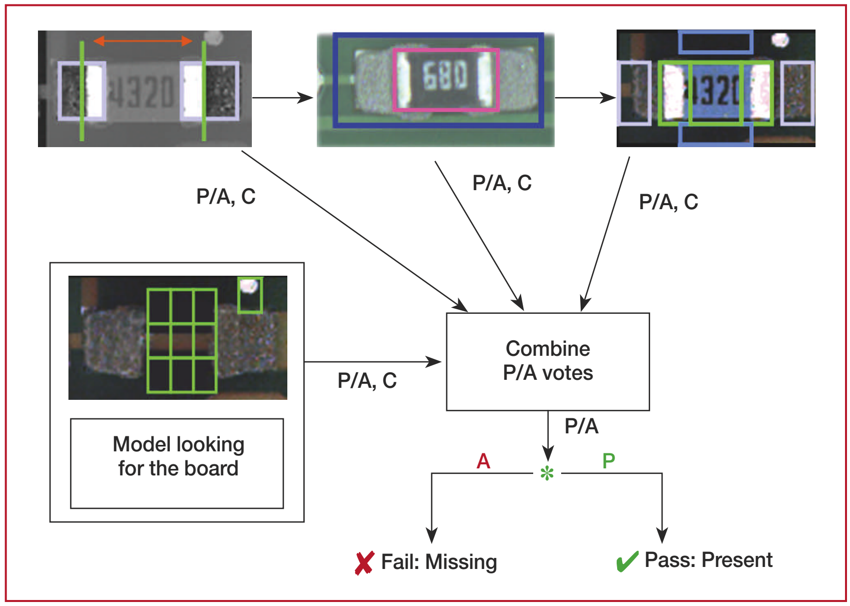


FIGURE 1. Separate software agents in an AOI system can look for the part's appearance, the part's structure, and the occlusion of the pads due to the presence of the endcaps. Other agents can look for the absence of the part (or the presence of the board). Each agent provides a decision on whether the part is Present or Absent as well as a Confidence measure. These votes can be combined to make a final decision.

Principle 2: Anticipating variations

The human brain never stops learning. With each new experience, it updates its world model, including tolerances on allowable variations. This ability allows the brain to anticipate variations in future inputs.

Translating this concept to AOI, a software agent could sample the board on every inspection in order to best understand the visual aspects of the parts and the board under test. The agent could handle changing conditions on an "inspection by inspection" basis rather than relying on learned or programmed conditions that may be no longer valid.

Furthermore, having the continuous data allows the system to look for trends of change and, in some cases, perform process control. **Figure 2** shows how an AOI system can adjust dynamically to sample the colors on every board by looking at predetermined locations that should contain the colors for various elements. The colors can feed into the algorithms that use them to ensure the algorithms have the right color palette for each board in the inspection process.

Principle 3: Examining data in context

Information that is examined out of context can be ambiguous. Consider an impressionistic painting, in which a paint daub that by itself just looks like a brown smudge is readily interpreted as a face when examined as part of the entire picture. This idea also applies to real-world image analysis. The brain ascribes great significance to context when interpreting images in the presence of noise and other imaging imperfections (Ref. 4).

(continued)

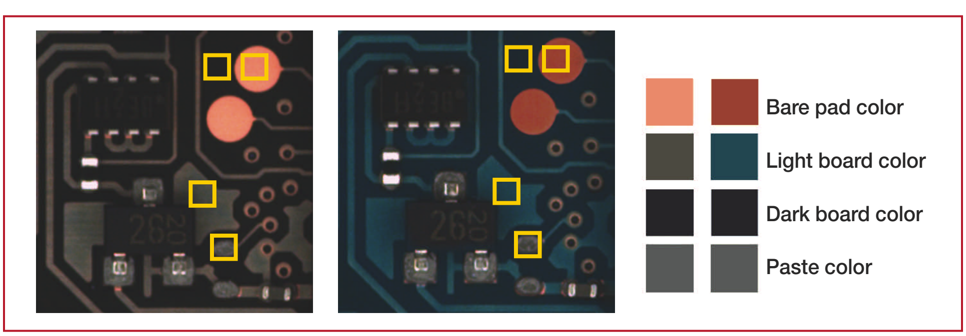


FIGURE 2. A PCB can be coarsely represented by just a few colors that often change across boards. This figure shows the basic color set for two boards of the same type.

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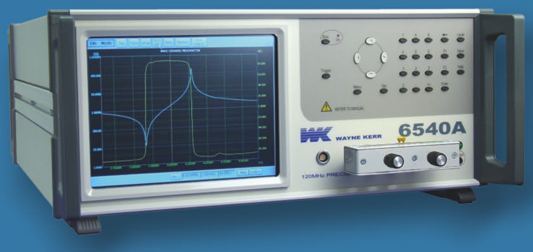

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It is widely known that there is a great deal of variation in how things look on a local level during the inspection of a PCB. Shiny parts have a range of luminances and colors and tend to reflect the image-capture system. PCBs have color changes in the mask across the board and over different substrates. In addition, the boards, parts, and paste change their color or their markings so frequently that it is difficult to tell based on local information whether the object is good or bad.

Dealing with these problems is simplified if an AOI system considers not just the local information but also the gestalt of the neighborhood. A device that looks like a smattering of colored pixels can be correctly classified when examined in the context of the pads and board around the device and the expected board underneath it. A rotated part that on its own does not stand out as a fault becomes plainly apparent when seen in relation to the parts around it (**Figure 3**).

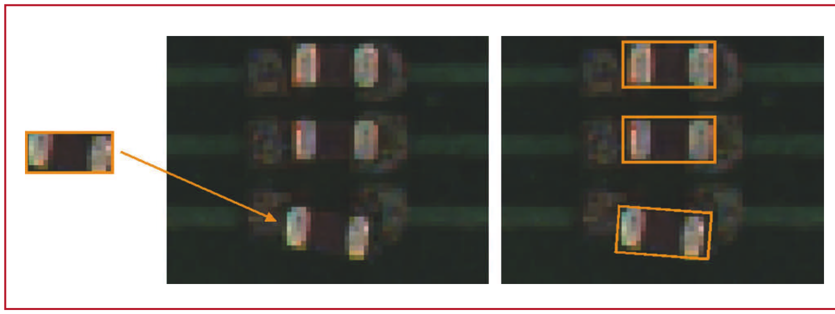


FIGURE 3. Without context, the 0201 device on the left looks correctly oriented. When the 0201 is examined with respect to other properly placed components, however, it becomes clear that the part is rotated.

Principle 4: Qualitative complements quantitative

Neurophysiological studies of cells in the visual cortex, the seeing part of the brain, suggest that many neurons encode image information far more coarsely than you might expect. A single neuron might indicate the direction of contrast over large regions (is the left side brighter or darker than the right?) rather than quantitative information like the exact location of an edge, its precise angle, or an exact color.

Why would the brain choose to throw away the fine metric data in favor of coarse relative estimates? It turns out that this is a clever strategy for building in variances. Inequalities are more tolerant to image changes than metric measurements. A representation built from qualitative codes, therefore, turns out to be more adaptable to imaging variations. A face lit in any of a number of different ways yields the same qualitative code, but very different quantitative codes (Ref. 5).

This is a valuable insight for AOI system design. Manufacturers often design their object recognition systems to look at fine details such as the precise transition between an object and its background or the interior transitions between luminance or color regions. These are known as "edges." Other systems look at the exact colors or luminances of different parts of the image.

But manufacturers could design their systems to make representations for acceptable components or faults on a PCB that are based on qualitative relations between regions. These representations are likely to be more robust across variations than those that include quantitative detailed information. **Figure 4** shows how a qualitative representation can be used to determine part presence or absence by looking for a part in relationship to other elements.

Of course, some quantitative information is undeniably useful, especially for process control. A challenge of AOI system design lies in figuring out a good balance between invariant qualitative representations and sensitive quantitative ones.

Principle 5: Prior knowledge combined with experience

Within a few months of birth, a human infant is proficient at localizing and even recognizing faces in complex scenes. What underlies such rapid learning?

One proposal suggests that evolution has equipped the brain of a newborn with a coarse face schema, which predisposes the infant to attend to patterns that are more likely to be faces. The resulting biased sampling facilitates the learning of faces (Ref. 6). This is an example of how the brain uses prior knowledge to bootstrap its learning and uses real-world experience to refine its concepts.

This strategy translates to AOI systems. Agents combine built-in knowl-

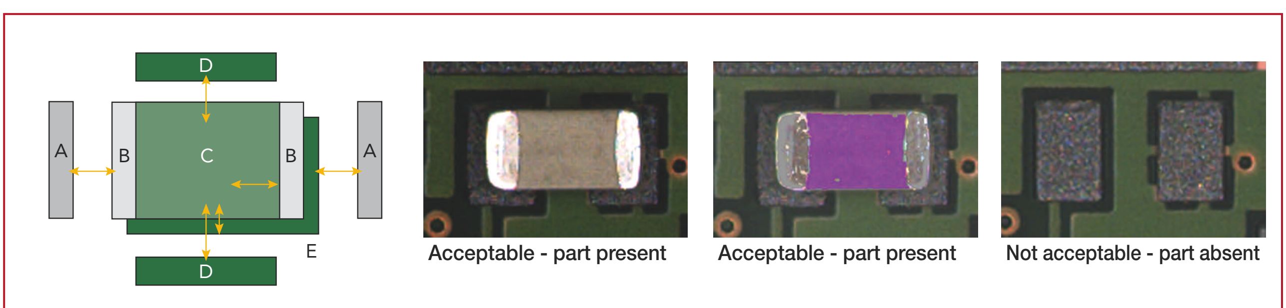
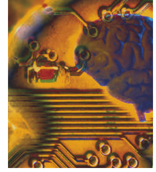


FIGURE 4. One qualitative model of a capacitor encodes regions where the endcaps are brighter than the body, the body is different from the endcaps, and the body is different from the background. This representation is satisfied when the endcaps are bright or dark, the body is brown or pink, and the board color changes. The representation correctly fails the image when the part is absent (right), because the endcap regions are not brighter than the paste, and the body is not different from the background.



edge about PCB inspection with learned data about the board under test. The knowledge gives the agents a base level of ability without user intervention. The learned data makes the agents experts for that particular board. The dynamic sampling for each inspection makes them even more adaptable to changing conditions. The result is consistently good inspections over long periods without significant human modification of the program. **Figure 5** shows an example of how an AOI system might combine built-in knowledge with learned knowledge.

A case study

Landrex and Imagen have tested these principles on a Landrex Optima 7200 preflow inspection system. Tests done in-house and at customer sites demonstrated that use of the five principles increased the system's performance over traditional techniques.

To understand how this works, consider an example of a capacitor whose endcaps often appear oxidized and whose body color changes from time to time. Imagine also that the board colors change from assembly to assembly.

A traditional system that has learned one appearance of the part and board may falsely fail a part when its appearance

AOI systems now "see" better and can process information in previously unimaginable ways.

changes, or it may accept a missing part as present when the board color changes. Such a system would have to learn multiple color options and combinations in order to adapt to the changing conditions.

In the 7200, if the part color changes, then from principle 1 (collective action), some models may fail the part or be uncertain about whether it is present. Other models, however, that look for structure or occlusion of the board will be strongly convinced the part is present. This is bolstered by the fact that one of the models uses the qualitative encoding from principle 4 to look for part structure and not part appearance, which is often invariant to color or luminance changes. *(continued)*

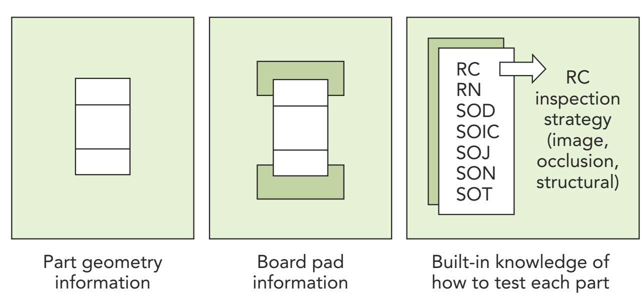


FIGURE 5. Built-in knowledge, including part geometry information, board pad information, and strategies for inspecting each known part type, can give an optical inspection system the ability to inspect parts on a PCB without ever having seen any real-world examples.

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Principle 2 (anticipating variations) allows the system to know the board color has changed from the sample board and to distinguish this from a part color or luminance change. Principle 3 allows the system to analyze the part in the context of the board and parts around it, thus, adding more information to the process. Principle 5 (prior knowledge) allows the system to tolerate variations by simply knowing a part is a capacitor; the engineer does not need to develop a complicated program to teach the system all possible variations and combinations.

In terms of false calls and false accepts, the 7200 is able to achieve three orders of magnitude performance difference (from 1000 ppm to 10 ppm) compared to traditional techniques, such as image comparison or edge detection. In addition, the system is able to run over large durations of time with little user intervention or changes to the program while still maintaining its low false call rate. For instance, at one customer site, the 7200 required only 15 discrete modifications over a two-week period of continuous use on roughly 5 million components. Once the modifications were made, there was no re-occurrence of the original issues.

Until recently, the capabilities of computers, cameras, and lighting were quite rudimentary, which constrained the types of images that could be collected and the processing that could be done. With the introduction of faster computers, cheaper memory, higher-resolution cameras with greater color capacity, and white LEDs, automated inspection systems can now "see better," and they can process information in previously unimaginable ways. In the coming years, as manufacturers apply the synergies between the principles of brain science and computer vision to their algorithms, the industry should produce robust inspection systems that are easier to program and that offer more accurate assessments of PCBs. T&MW

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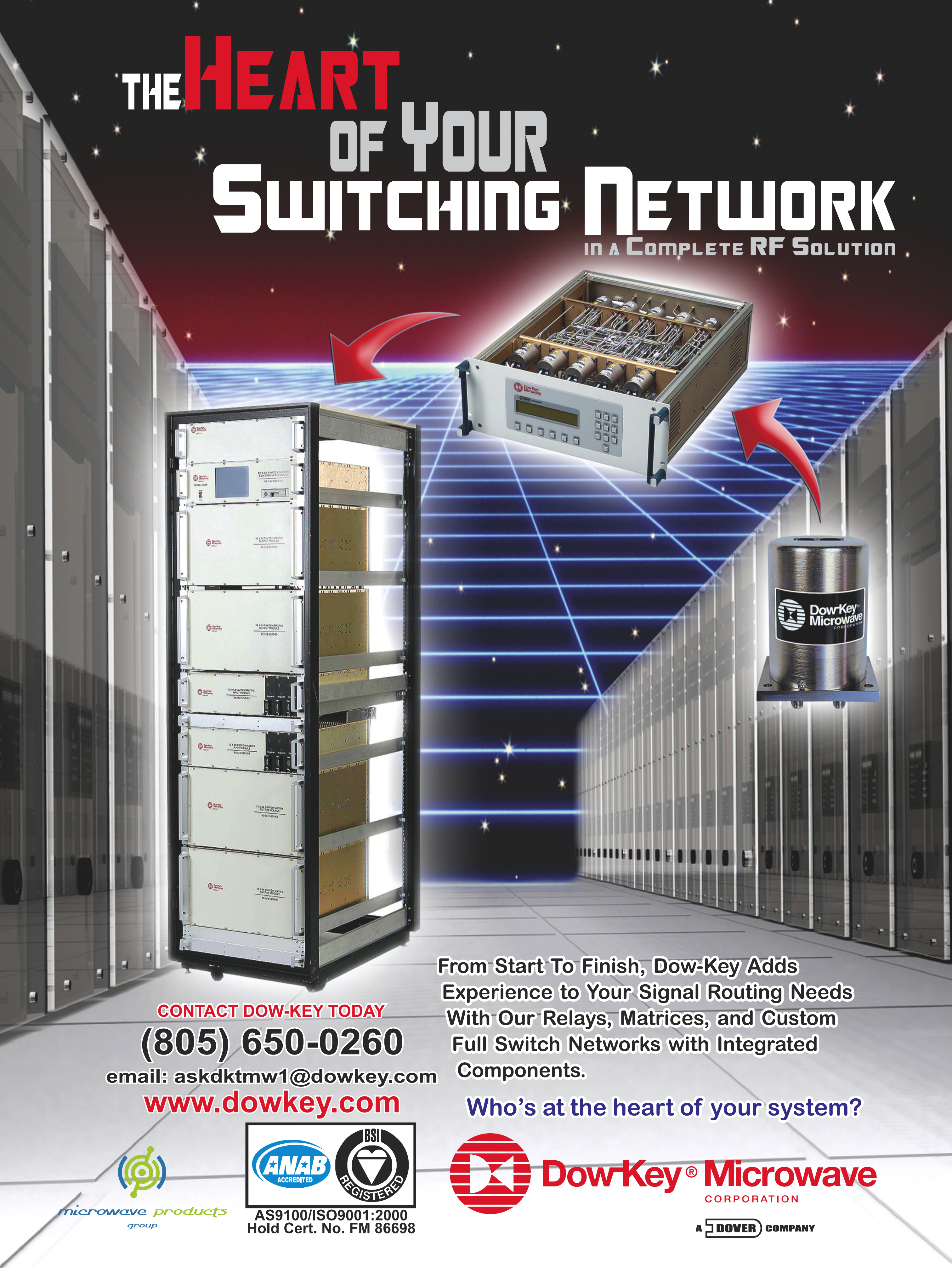
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Companies in the aerospace and defense industries use equipment for dozens of years, and these line-replaceable units (LRUs)—such as radar, radio, and positioning systems—require test and calibration throughout their lifetime. Yet, building a test system that will serve an LRU for its entire life is a nearly impossible task.

While test equipment has a longer life span than, say, PCs, an instrument is likely to need replacement before an LRU is taken out of commission—but after the manufacturer has ceased producing that particular model. Thus, engineers often must replace obsolete test equipment with different models, and such replacements usually require software changes to both the test system and the test itself.

IEEE 1641-2004, "IEEE Standard for Signal and Test Definition," addresses the problem by defining a structure for test signals that makes software portable among equipment (Ref. 1). By employing the IEEE 1641 structure, you can replace a piece of test equipment with minimal impact on a test system.

The IEEE 1641 structure may also be the basis for synthetic instruments, which use analog-to-digital and digital-to-analog converters (ADCs and DACs) to provide the functionality of multiple test instruments. With the structure, you can also develop simulations, which are useful during product design. IEEE 1641 is also incorporated into other software standards, such as Automatic Test Markup Language (Ref. 2).

What is IEEE 1641?

IEEE 1641 lets you define signals purely in terms of the LRU under test, which makes it easier to replace instruments in a test system and makes the system itself more resistant to obsolescence.

You can define test signals by connecting Basic Signal Components (BSCs), which form the basic building blocks of any test signal; their attributes let you define a test signal. The main groups of BSCs are sources, conditioners, events, measurements, digital, and connections. A Test Signal Framework (TSF)

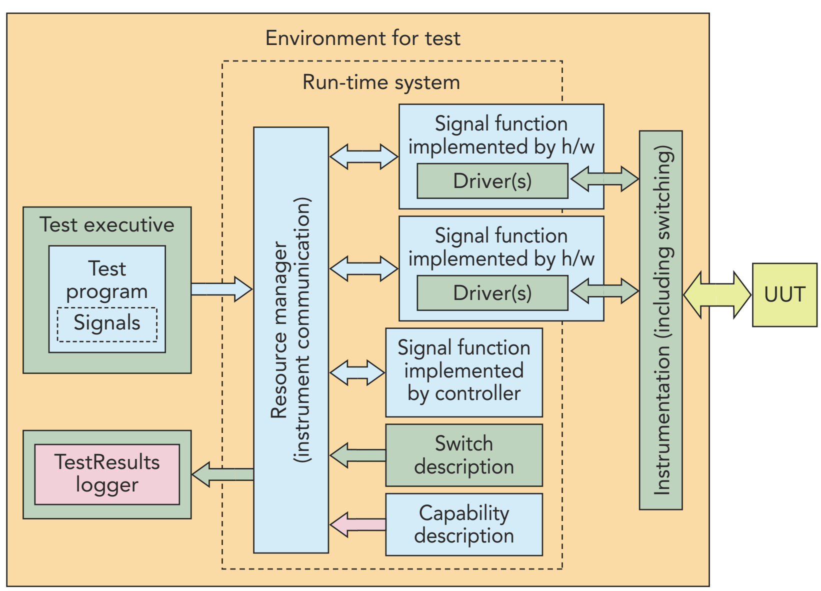


FIGURE 1. A resource manager is the intermediary between signals and instrument drivers.

is a high-level grouping of BSCs designed to provide a reusable block of signal functionality.

A mathematically based Signal Modeling Language (SML) lets you precisely define the signals within a BSC. You can use SML to form a complete functional model of a signal. Thus, you can use it with traditional test instruments or synthetic instruments to create live signals, or you can use it for simulations (virtual signals).

You can arrange BSCs and TSFs together to form a complete test signal, known as a signal graph. You can define signal graphs either graphically or through text. If you use text, use Extensible Markup Language (XML), which is both machine readable and easily formatted for human reading.

You can also use Interface Definition Language (IDL), which lets you create a standardized programming object such as an ActiveX object to represent a signal graph. You can then call the object from most common programming languages.

Because IEEE 1641 defines signals as they relate to an LRU, you need a way to translate the signal definitions onto physical signals. You can use a resource manager to map the BSCs and TSFs to a system's instruments and route signal data to the instruments through drivers. **Figure 1** shows the resource manager as the intermediary that maps signal definitions to instrument drivers. "Implementing IEEE 1641," p. 48, outlines the steps required to put IEEE 1641 into practice.

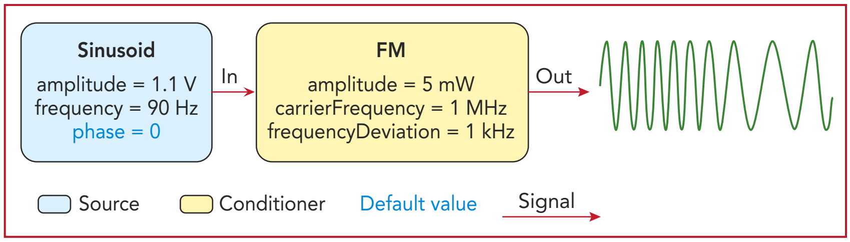


FIGURE 2. A BSC for an FM signal consists of a signal source and a signal conditioner, both of which contain attributes of the signal.

The details of Basic Signal Components

BSCs contain the attributes that control the behavior of a signal. Examples of AC-signal attributes are amplitude, frequency, and phase. A BSC for an FM signal could consist of a signal source and a signal conditioner (**Figure 2**). Both the source and the conditioner have attributes that define the FM signal, such as amplitude, frequency, and frequency deviation.

Some commercial software programs offer a library of BSCs that can make it easier to construct an IEEE 1641-compliant test program. Compliant programs assign default values to the attributes in the BSCs, which simplify your work even further. For example, the phase attribute of a sinusoid is frequently not important and you can ignore it. The default value for amplitude is zero for safety reasons. An unexpected output from a device where amplitude has inadvertently not been specified could cause damage or injury. Attributes can also have default units. For example, a sinusoid's frequency has hertz as its default unit. You can, though, specify a signal's frequency as a period in seconds instead.

BSCs also have "In" connections between them. The "In" connection applies to a signal passed to one BSC from another. An exception to this rule is made for the case of Carrier, where you must distinguish between the modulating signal and the carrier signal. Usually, no such distinction is required, as in the case of summing several signals. An "Out" connection defines the output of the complete signal, which should be applied to, or measured from, a pin on the LRU under test.

Just as BSCs can define signals, they also can define events. Thus, you can use events to synchronize or "gate" physical signals. For example, you can gate a sinusoid (used as an RF carrier) with a clock to produce RF bursts as part of a radar signal.

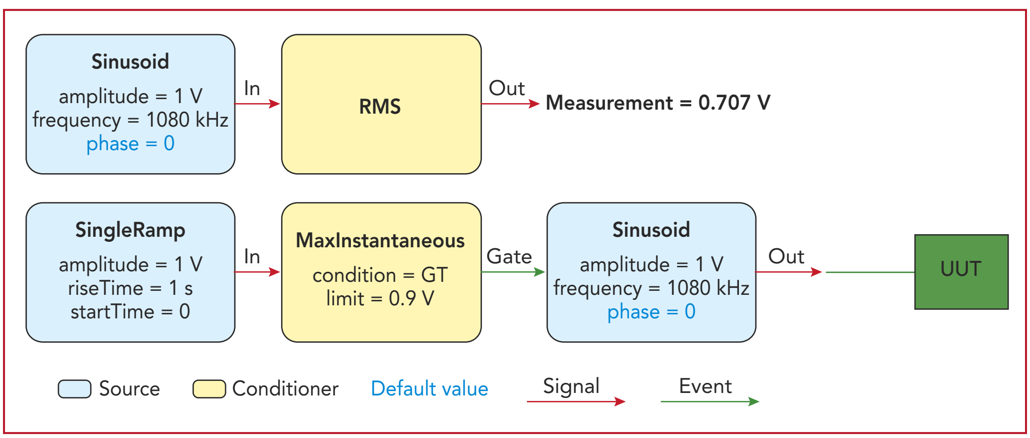


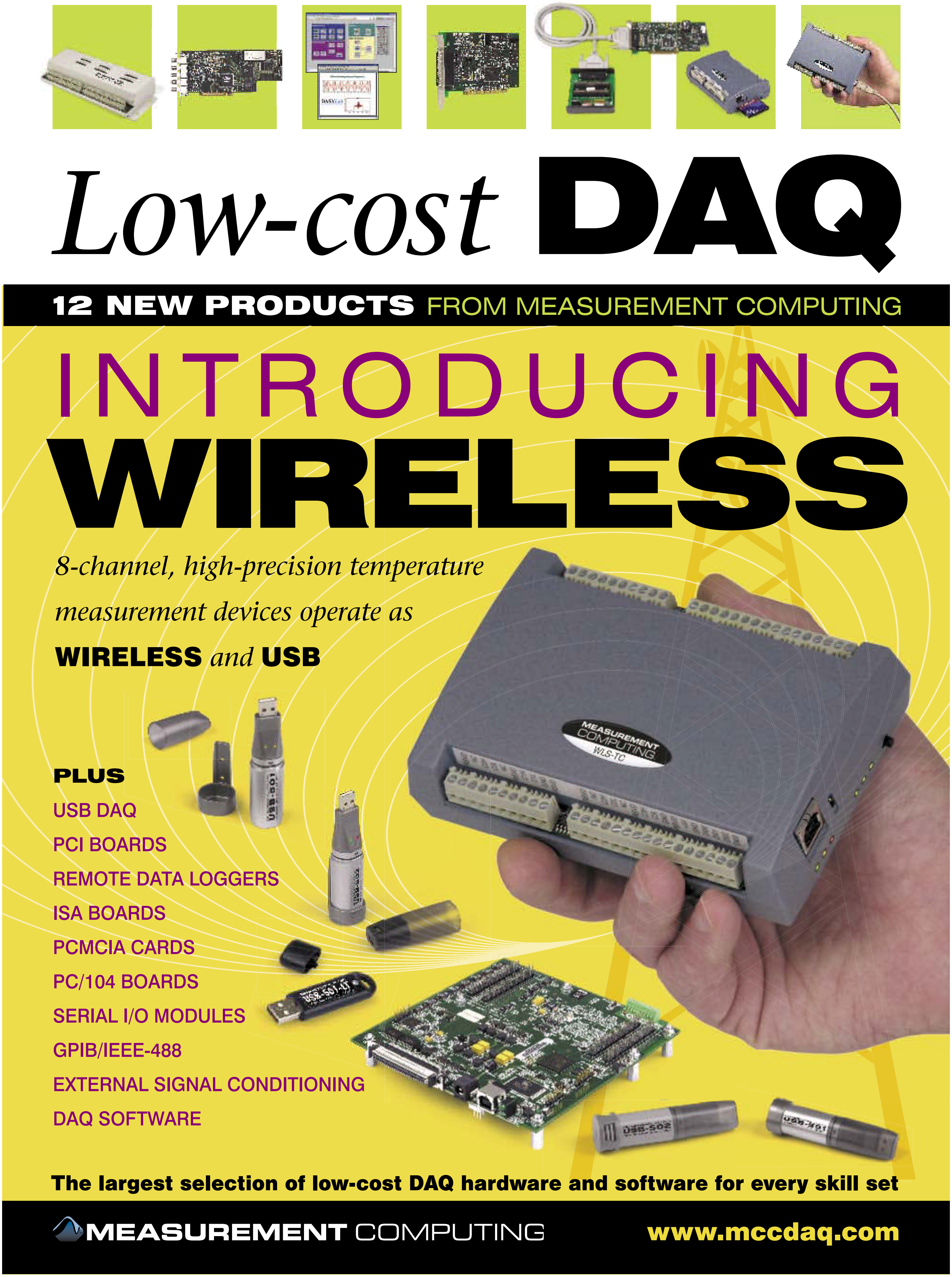
FIGURE 3. BSC components have "In" and "Out" attributes that model signal paths within the BSC.

Tests require measurements

Measurement BSCs can be set up to let instruments capture signals and produce a required value, such as RMS or Peak (**Figure 3**). BSCs can also compare a measured value with upper or lower limits to yield a pass/fail result. They also raise an event for use as a gate or for synchronization when a particular condition is met.

Digital BSCs include logic levels, data rate, and clock rate. They address the digital characteristics of the signal, such as the voltage for a logic 1 (5 V) and a logic 0 (0 V). Don't, however, confuse these nominal voltage levels with the "analog" attributes of digital signals such as rise time and overshoot.

To create connections between signal graphs and the physical test points on an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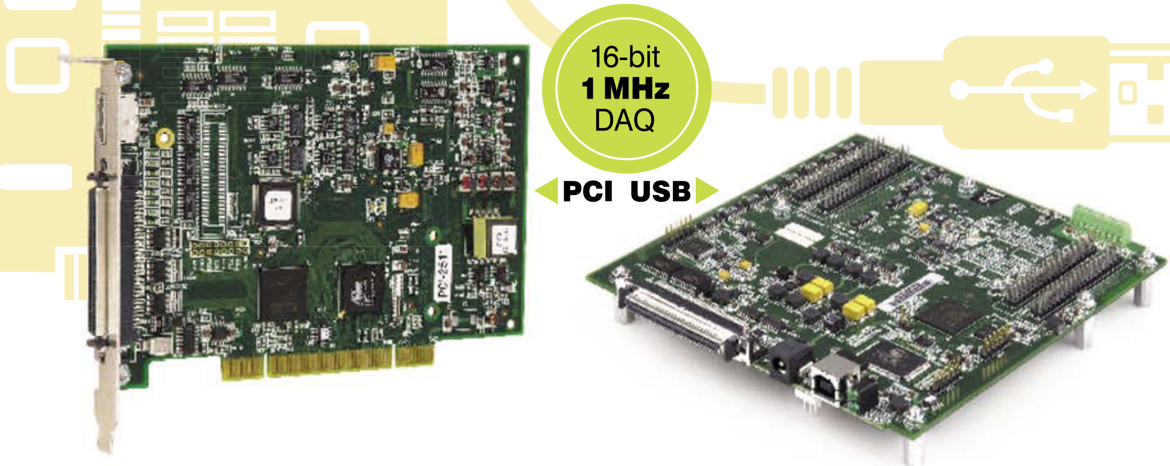

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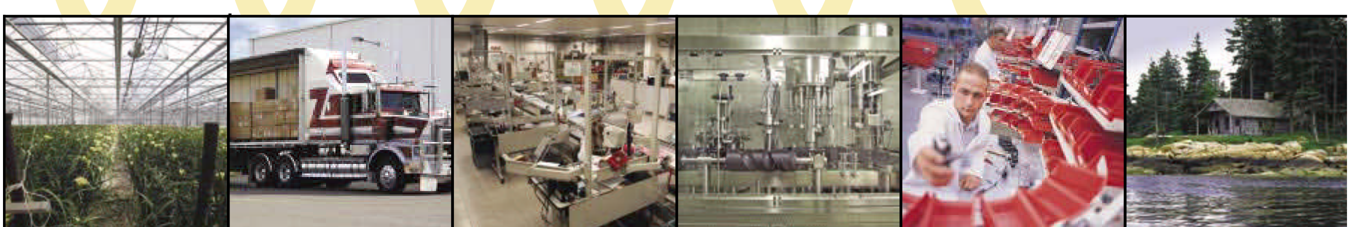

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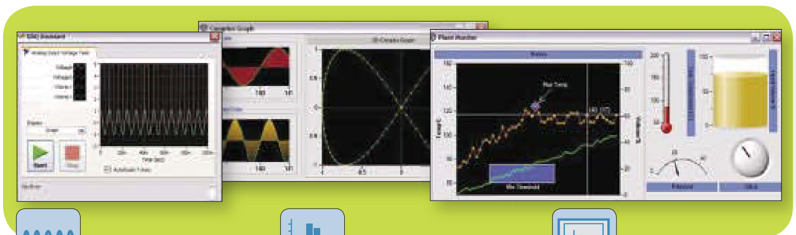

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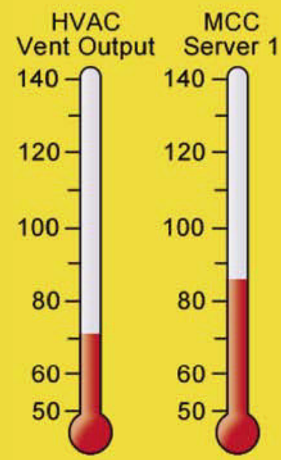

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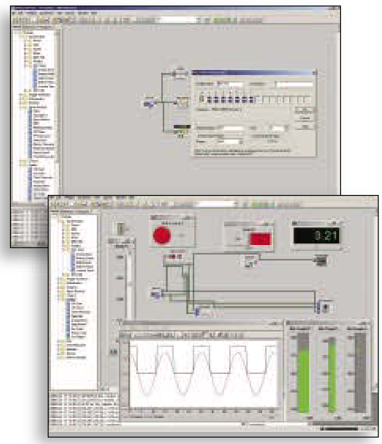

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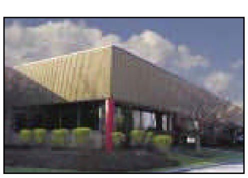

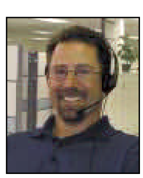

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LRU, you can use connection BSCs. A connection BSC's attributes are typically pin names that describe a contact within a connector on what would commonly be the unit under test (UUT). Once you define your signal model using BSCs, you can create a TSF. **Figure 4** illustrates two radar TSFs.

The SML description of signals contained in BSCs and, thus, TSFs lets you build a signal that accurately simulates and generates waveform data. You can use SML to verify signals or produce waveform data for synthetic instrumentation.

SML is not, however, readily interpreted at a rate sufficient to meet many real-time applications. Simulations produced using SML are effectively static.

Streaming signals

IEEE 1641 lends itself to a streaming framework that provides an efficient method of dealing with complex signal definitions. A common example of streaming is in multimedia systems, such as MPEG data pipelined between "filters" that decode a data stream, split the stream into audio and video streams, and render these video and sound streams to the screen and speakers.

Filters are the streaming equivalent of BSCs, and a filter graph is directly analogous to a signal graph. Coding of BSCs as streaming filters, through an existing framework such as DirectX, provides a system for simulating and synthesizing changing signals using ADCs or DACs.

The streaming framework lets you produce and measure dynamic signal data and plot the results. With most current PCs, you can simulate, but not reproduce, a real-time signal up to about 4 MHz.

With streaming, you can use a PC sound card to test communication headsets and telephony devices. Recently, PCI Express instrument cards brought fast DACs and ADCs to a faster data bus.

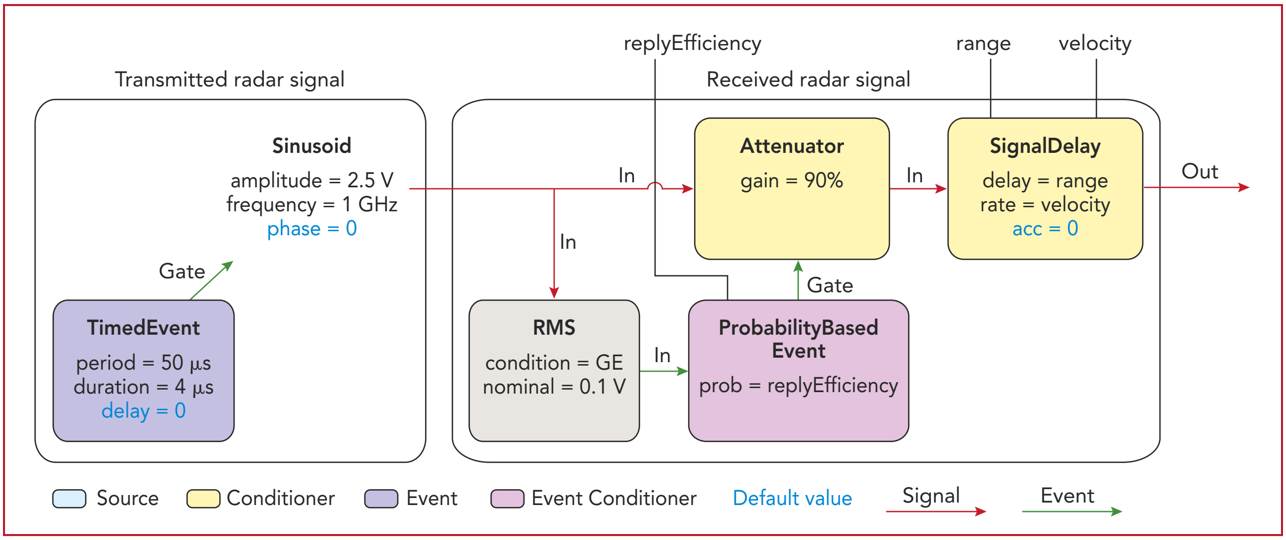

FIGURE 4. These two TSFs, which handle transmitted and received radar signals, are formed from BSCs.

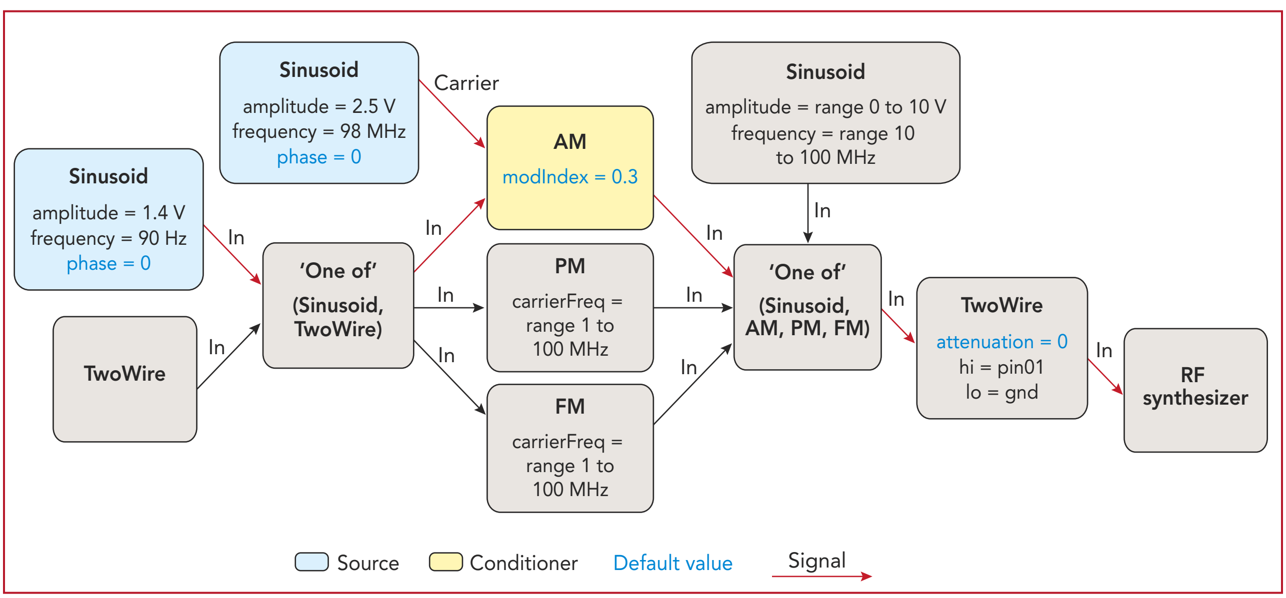

FIGURE 5. This resource description of an RF synthesizer was constructed from signal graphs that contain BSCs.

Implementing IEEE 1641

By following these steps, you can create a tester that complies with IEEE 1641:

1. Define a signal in terms of BSCs and TSFs.
2. Compare a signal definition with the resource description that a resource manager holds for the test system.
3. Load drivers as resources are matched to signals.
4. Match connection BSCs in a pin map and load a driver to control the system routing and switch configurations.
5. Allocate signal functions from a software library that can be implemented on the system controller.
6. Log measurements and test results in XML format.

Signals above 1 Msample/s can be generated live and on-the-fly from IEEE 1641 test programs through the streaming framework.

Many applications, however, require more accuracy and precision than a PC sound card or data-acquisition card can produce. For those applications, you could use an arbitrary waveform generator and a digitizer.

When you reproduce an IEEE 1641 signal-graph within a streaming-filter framework, you can transform signal definitions into signal data. By rendering this signal data visually, you can create a simulation against which you can verify a signal definition. Typically, a simulation requires points of reference and measures of scale, such as the voltage, frequency, and time scales found on oscilloscopes and spectrum analyzers.

Using BSCs to create resource descriptions creates a common interface between test programs and instrumentation. **Figure 5** shows a signal graph that describes a test resource (an RF synthesizer).

Typically, a resource manager views the definition of the test signal and maps it onto a list of descriptions it carries for the instrumentation. Here, the XML defined in the standard becomes useful. Because XML is well structured and supported by software tools, you can easily parse data to find a match between the signal definition and the resource description.

IEEE 1641 test programs fully define the signals you must apply to, or measure from, an LRU. Thus, you have available all the information you need to source new instrumentation. Furthermore, SML enables simulations that provide validation that the output or measurement from a replacement instrument meets your requirements.

That said, many instrument-replacement programs falter because test specifications aren't described rigorously enough. For example, a replacement instrument with an improved frequency response may seem to be a "better" choice. Unfortunately, an unspecified (or, more likely, unconsidered) part of the test might have been to filter off high-frequency harmonics. Now that they can be measured, the test fails.

IEEE 1641 does not force you to rigorously specify all of the details in a test program, but it does enable you to specify the attributes that improve obsolescence management. Of course, as in all cases, you still need good engineering practices to be assured of success. T&MW

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1. IEEE 1641, "IEEE Standard for Signal and Test Definition," IEEE, Piscataway, NJ. 2005. www.ieee.org.

2. Automatic Test Markup Language (ATML) project information, IEEE, Piscataway, NJ. grouper.ieee.org/groups/scc20/tii/.

Matt Cornish *is a principal consultant at EADS Test & Services, where he has worked for eight years. He leads a small team developing automated test systems and test program set software tools and is an active participant in the IEEE ATML and Signal & Test Definition working groups. He has published papers on the subject for the annual Autotestcon conference. Matt.Cornish@eads-ts.com.*

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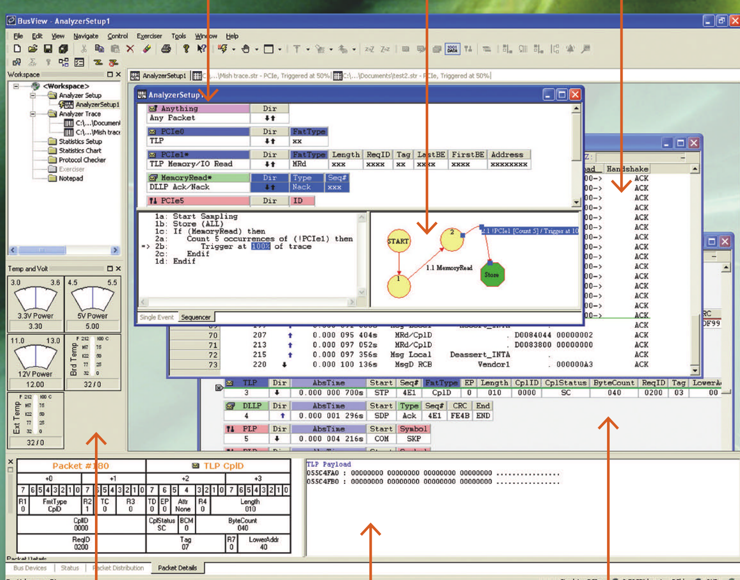

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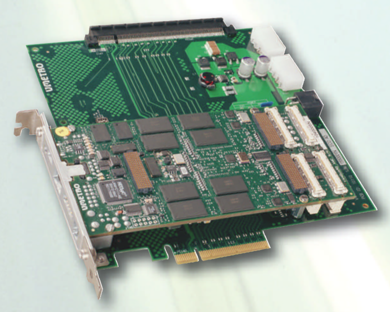

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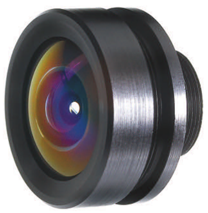

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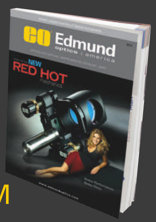

MACHINE-VISION & INSPECTION

TEST REPORT

Smaller inspection firms find a niche

Steve Scheiber, Contributing Technical Editor

The printed-circuit-board inspection industry is dominated by a handful of major competitors that get most of the attention. Smaller companies cannot establish an identity in the marketplace simply by being like the "big boys." Instead, they have to offer features and capabilities, service and support, or price advantages that set them apart.

YESTech in San Clemente, CA, epitomizes this "can do" attitude. I recently discussed the challenges facing smaller firms with Don Miller, the company's president and co-founder.

Q: How does your approach to the marketplace differ from that of your competitors?

A: We try to look at the inspection task from the point of view of the customer. If the technology we offer doesn't meet the customer's needs, then it can't be the right solution. If all we do is mirror the offerings from the industry leaders, then the customer has no incentive to choose us instead.

INSIDE THIS REPORT

Q: Do you plan to continue to develop both automated optical inspection (AOI) and x-ray products?

A: Some of our competitors believe in a healthy growth of automated x-ray inspection (AXI). They have much more modest expectations about AOI. Our AOI lines have been very successful, and we are applying what we have learned to our more recent entry into x-ray inspection.

Q: What do you do differently?

A: More than anything else, we try to make our systems user-friendly and adoption-ready so that people can get them up and running on the manufacturing line quickly and easily. For example, we provide a visual front end that users find more intuitive for designing an inspection regimen than they find wrestling with conventional programming code to be. As a result, our inspection systems offer advantages to contract manufacturers and others where high-mix, product changeover, and program creation are the gating items. We expect operators to be able to create a complete inspection program in 30 min—a far cry from the days of work that a code-based program often requires.

Q: How do you achieve such fast results?

A: We start with a standard device-package library to simplify training and ensure program portability across manufacturing lines. We also rely on PCs and other technologies that users are already familiar with.

Don Miller
President and Co-founder
YESTech
Courtesy of YESTech

Q: What other advantages do you offer?

A: It often filters down to price, but if you look more closely, it is our flexibility. We can provide custom software solutions or honor other requests on the turn of a dime. I can do in a couple of staff days what takes the big guys months. We stand out in front of the curve, anticipating our customers' needs. We are not tied to our own intellectual property or standard systems. Big companies get patents. We provide other services.

Q: What are your plans for the future?

A: For one thing, we are looking to expand geographically. We're a relatively new company, founded only in 2002. Until now, we have concentrated most of our efforts in North America. But the emerging and fastest growth markets are in India and China and elsewhere in Asia. We've done well there with manual x-ray systems, but we are only now beginning to expand into automated x-ray. We also plan to expand further into high-volume applications. As our company grows, we become better able to take proper advantage of these enormous opportunities. □

EDITOR'S NOTE

"Standard" doesn't mean "stagnant"

Steve Scheiber, Technical Editor

Creating a standard has inherent challenges. In the early days of the test industry, test and inspection equipment relied on custom I/O buses. No bus provided a perfect solution, but developers could adjust their features and capabilities to match a specific need. Standard alternatives, such as GPIB and VXI, of necessity represented compromises among the individual requirements of the participants. These standards have subsequently had to evolve to keep pace with technological changes.

Two articles in this issue of the "Machine-Vision & Inspection Test Report" examine aspects of establishing a standard. "New standard improves verification of Data Matrix codes" explores what happens when the conditions that a standard addresses change. The original standards for verifying Data Matrix codes assumed manufacturers were printing black ink on white labels. As direct-part marking has become more common, this assumption no longer makes sense.

"GigE Vision makes strides" looks at factors you must consider when implementing the GigE Vision standard. For all the talk about "plug-and-play," you still need to make decisions about network interface cards and frame grabbers.

Standards are not panaceas. They are merely tools that can help us do our jobs more easily. Bending them for your situation still requires considering their limitations as well as their advantages. □

Contact Steve Scheiber at sscheiber@aol.com.

HIGHLIGHTS

MVTec opens US office

On January 1, Munich-based MVTec Software opened a division in the US. Based in Cambridge, MA, the new division (MVTec LLC) will support the company's distribution partners in North America.

MVTec Software products include Halcon and ActivVision Tools. Halcon provides a library of operators for blob analysis, morphology, pattern matching, and metrology. ActivVision Tools helps engineers develop machine-vision applications without the need for programming.

"Primarily, MVTec LLC will assist our distributors in their customer support, but at the same time it will impart knowledge about this complex technology," says Dr. Heiko Eisele, president of the new company.

"We received a lot of inquiries from US system integrators looking for standard solutions in 3-D robotics for on-site production," said Dr. Olaf Munkelt, managing director of MVTec Software in Munich. "Thus, it is high time to expand our customer base in the USA and Canada." www.mvtec.com.

GKS expands on-site services

GKS Inspection Services has enhanced its Detroit-area dimensional inspection and metrology services with the addition of a third Faro portable CMM articulated arm. With the new arm, GKS can better handle the increased interest from customers for on-site inspection and reverse engineering services. GKS selected the largest Faro model to be able to measure large parts, which are common in the area's automotive industry. The 12-ft platinum Faro arm is equipped with both a touch probe and a 3-D laser scanner. www.gks3d.com.

RedShift Systems relocates

Thermal imaging supplier RedShift Systems has moved its headquarters to Northwest Park in Burlington, MA, to accommodate anticipated growth. The company's new headquarters include significantly expanded laboratory space for thermal camera testing, as well as dedicated facilities for RedShift's advanced characterization and calibration systems. www.redshiftsystems.com.

Nordson to buy x-ray system maker

Nordson, a producer of precision dispensing equipment that applies adhesives and coatings to products during manufacturing, has agreed to acquire Britain's Dage Holdings, a manufacturer of test and inspection equipment used in the semiconductor and printed-circuit-board industries.

Dage's digital x-ray systems and bond testers analyze the integrity of electronic connections in semiconductor packages and printed-circuit-board assemblies and ensure quality and process control during the manufacturing process. The company employs more than 200 people and had revenues of approximately $59 million during the 12-month period ending October 31, 2006.

"The purchase of Dage fits Nordson's strategy of acquiring companies with above-average growth in markets currently served by Nordson companies," said Edward P. Campbell, chairman and CEO of Nordson. "Over the three-year period ending April 30, 2006, Dage revenues and operating profit grew at annual rates of 24% and 69%, respectively. These growth rates are nearly identical to those of Nordson's Advanced Technology Systems segment, which since 2003 has grown revenues and operating profit at annual rates of 23% and 59%, respectively." www.nordson.com.

New standard improves verification of Data Matrix codes

Steve Scheiber, Contributing Technical Editor

When creating any standard, certain "rules" apply. A standard must incorporate some features critical to every company that adopts it, but inevitably, every company will identify critical features that the standard lacks. As a result, standards must evolve as relevant information changes and as user experiences reveal their shortcomings. The standards for verifying the Data Matrix codes that are used to identify parts for inspection illustrate these principles perfectly.

Currently, three standards are used to determine the mark quality of Data Matrix codes—ISO 16022, ISO 15415, and AS9132 (Refs. 1–3). ISO 16022 is the 2-D symbology specification. It describes how to construct a Data Matrix code, and it guides developers in generating software algorithms that read the code itself. The initial release also included an appendix that defined mark quality metrics.

Essentially, the standard covers how to encode the information, how to decode it when you read it, and how to verify that it is correct. The standard assumed, however, that codes consisted of black marks applied to white labels (rather than directly to a part), and it included no measurable quality standards.

When a product is destined for military or other high-reliability applications, manufacturers need criteria for ensuring that a Data Matrix mark will be readable throughout the product's life—heat, friction, and other indignities notwithstanding. ISO 15415 was developed with the intent to provide a verification standard for demanding applications. Like 16022, this standard assumes that all images consist of black marks on white paper labels. It includes only a single lighting configuration, and the calibration routine limits the system to a fixed exposure and fixed gain for image analysis. If you adhere to the requirements, you will find that many codes that an ordinary person can read easily will fail an automatic verification system.

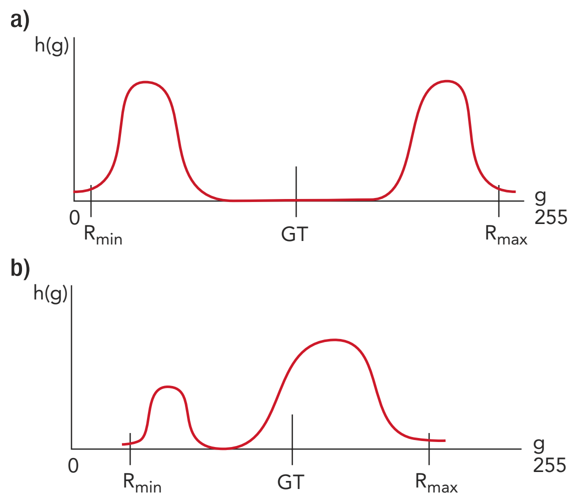

Fig. 1 **a) The old verification standard expected black marks on white paper, producing matched peaks near 0 and 255 on the 8-bit gray scale. b) Marking directly on the part produces marks that peak a considerable distance from 0 and 255, making verification more difficult.** Courtesy of Cognex.

When using an 8-bit camera, each pixel will have a value from 0 (100% black) to 255 (100% white). The histogram of a well-formed black-on-white code will have two distinct peaks. One peak should have a normal distribution near 0. This peak will represent all the pixels from the black cells. Another peak closer to 255 for the white background should also have a normal distribution (**Figure 1a**).

Yet, as companies increasingly turn to using direct part marking (DPM), the appearance of marks is becoming much less uniform. Data Matrix marks are imprinted using a variety of methods, so their color and shape can deviate considerably, and the variety of surfaces and materials on which they are imprinted rarely provides a uniform white background. **Figure 1b** shows a more realistic high-contrast hologram, where the mark is less than black, the background is other than white, and the peaks are not equal.

Although many companies follow ISO 15415 for paper-based Data Matrix codes, companies that use dot-peen, laser, or electrochemical-etch marks have to conform to AS9132. Created by the SAE's International Aerospace Quality Group, this document describes how to make the marks. It was never intended to address camera-based verification of a mark. It outlines no measurement method, no lighting configuration, and no assurance of consistency in the way that companies implement its provisions.

Carl Gerst, director of ID products for Cognex, noted, "When people mark parts by laser-etching, dark elements tend to be larger than light elements. CO_2 lasers will 'over burn' during the marking process. According to AS9132, overmarking dark cells by as little as 5% will produce a verification failure."

Because of the shortcomings of the early standards, Cognex and other imaging companies, working with the Association for Automatic Identification and Mobility (AIM), have prepared a new specification, which the

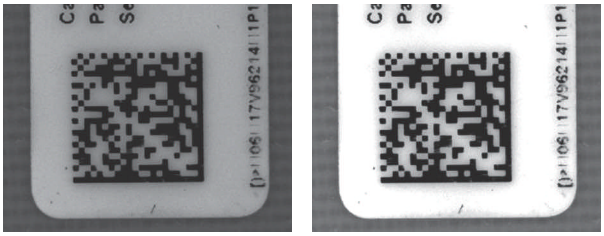

Fig. 2 a) Marks that would fail ISO 15415 verification will produce much better results using b) the techniques defined in the new AIM standard. Courtesy of Cognex.

Department of Defense intends to adopt. It "explains how to both specify and report quality grades in a manner complementary to, yet distinct from, the method in ISO/IEC 15415." (Ref. 4.)

The new Quality Guideline is more flexible and realistic than ISO 15415, as its specifications are independent of the marking method. Whereas 15415 permitted only one lighting configuration, the new standard specifies four:

• a diffuse perpendicular (on-axis/bright-field) setup, which illuminates the symbol with diffuse light incident at a 90° angle;

• a diffuse off-axis setup, which illuminates the object from below and is effective on curved surfaces;

• a low-angle, two-direction technique that aims light at the part at an angle of 30° ±3° from two sides, illuminating the symbol area with uniform energy; and

• a low-angle, four-direction technique in which the center of the beams from opposing pairs of lights are coplanar, and the planes remain at right angles to each other.

The new standard also outlines a method for setting the optimal image brightness, allowing a range of exposure and gain settings. Gerst said, "One concern with the AIM DPM standard is that because you can adjust exposure and gain, you could theoretically crank the system up to infinity. To avoid this, the document limits the combined increase in exposure and gain to 16X." **Figure 2** compares images captured using 15415 and the AIM standard.

Using DPM to identify products undergoing inspection represents a considerable improvement over paper labels that can become defaced or can fall off. The implementation of the new AIM DPM Quality Guideline should help manufacturers improve their ability to apply Data Matrix marks in a consistent method and make verification of the marks both easier and more reliable. □

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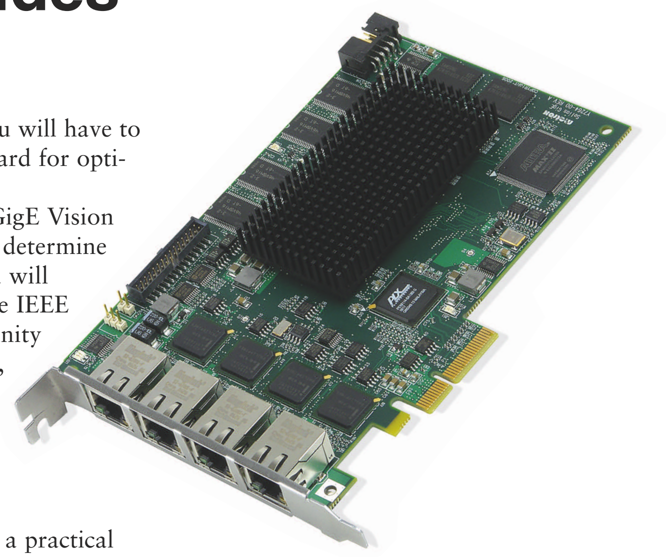
GigE Vision makes strides

Steve Scheiber, Contributing Technical Editor



Developers of GigE Vision systems should specify a network interface card that is designed for high-bandwidth applications. Courtesy of Matrox Imaging.

High-speed vision standards offer numerous advantages, but the standards themselves represent only a means of communication. Success in implementing them depends on understanding the tasks they perform and the equipment that supports those tasks.

In November, Matrox Imaging introduced its first interface card that incorporates the new Gigabit Ethernet (GigE) Vision standard. Recognizing the considerable buzz surrounding the standard, product manager Dwayne Crawford declared that the launch "allows customers to take advantage of the latest technology in the most optimal fashion."

I asked Crawford about the challenges that a manufacturer would encounter when implementing the standard for the first time. He noted that the industry is touting GigE Vision as the up-and-coming technology that will eventually dominate the market but that the critical issues have not changed.

"Regardless of the standard deployed in an application," Crawford said, "machine-vision developers must choose their components carefully." He added, "We expect most of the new GigE products to be released in the foreseeable future will be cameras."

Network interface cards

Although cameras that conform to GigE Vision will connect to any standard network interface card (NIC), some NIC models work with high-bandwidth cameras better than others. Crawford recommended that users look for an interface card that supports jumbo frames, interrupt throttling (sometimes called moderation), and receive descriptors (see "Choosing a network interface card for GigE Vision," on the next page). Furthermore, because GigE Vision is more complex than its conventional Ethernet predecessor, you will have to configure the interface card for optimum performance.

Before developing a GigE Vision application, you should determine how many I/O lines you will need. As engineers in the IEEE 1394 (FireWire) community have already discovered, most typical NICs lack auxiliary I/O.

Although accessing system I/O on the camera itself rather than on the frame grabber offers a practical alternative and proves equally effective, the camera may not possess enough I/O lines for your application. More importantly, the camera's decision-making capability is often limited. Crawford cited one example in which "a camera could not report to an application that a trigger had been missed because pulses were spaced too close together."

When selecting components, you should also evaluate the application's image-processing requirements. Standard NICs often cannot cope with CPU-intensive preprocessing tasks such as filtering, color-space conversions, and transformations. Instead, many users incorporate specialized frame grabbers into the process to execute these tasks.

Camera description file

The GigE Vision standard characterizes camera functionality according to the camera's end use. Some processes require control of the image size, while others demand acquisition and trigger controls, digital I/O, and analog controls.

Within each of these categories, the GigE Vision standard flags each permitted feature as mandatory, recommended, or optional. Out of the approximately 180 standard features, only a handful are mandatory, although most are recommended.

Aside from the technical specifications, what will distinguish one GigE Vision-compliant camera from another? How can you select one that suits your needs? Crawford summed it up succinctly, "Everything depends on the extent to which a particular camera implements the standard feature list."

GigE Vision requires that all camera features be described in a "camera description file" that follows XML syntax. As long as a vendor describes a feature adequately through the XML file, the end user can exercise complete control over it. When an application or driver parses the camera's XML file, it retrieves the machine-readable equivalent of the camera's "instruction manual."

The GigE Vision standard dictates that for a camera to be considered compliant, its XML file must support the appropriate mandatory features. Many cameras also exhibit a list of optional features. A truly compliant setup will implement the standard feature list in such a way that a camera from one vendor can easily be replaced with one from another—a real plug-and-play solution.

For machine-vision developers to successfully implement GigE Vision, they must understand its benefits and limitations. They must also consider the extra costs associated with additional I/O lines and with alleviating the burden on an overloaded CPU.

Crawford summarized, "Developers should buy their cameras from a reputable vendor, and they should seek out an NIC vendor who understands and addresses the unique challenges of the machine-vision industry. But hardware and software go hand-in-hand. A software environment that implements the standard feature list and incorporates custom features as well will enjoy the greatest acceptance in this competitive marketplace." □

FOR MORE INFORMATION

The GigE Vision standard is administered by the Automated Imaging Association. It was officially introduced in May 2006. www.machinevisiononline.org.

The GigE Vision specification relies on the GenICam standard to describe the features supported by a compliant camera. GenICam is a generic programming interface that is administered by the European Machine Vision Association and supports cameras for various buses. www.emva.org.

Choosing a network interface card for GigE Vision

When you are setting up a machine-vision system based on the GigE Vision standard, Matrox recommends that you look for a network interface card (NIC) that supports:

Jumbo frames—Jumbo frames are GigE data packets that hold more than the standard 1500 bytes. Setting the NIC's jumbo frame size to a large value improves GigE Vision's performance, because each packet can transfer more data, so the transfer process interrupts the CPU less often.

Interrupt throttling—The interrupt throttling feature allows the NIC to delay interrupting the host system until a specified number of events have occurred. The NIC then interrupts the CPU only once and transfers all queued events. This feature means that the host system does not have to service an interrupt for every packet received.

Receive descriptors—Receive descriptors are software metadata that the NIC associates with data packets that it buffers in memory. The more receive descriptors that an NIC has available, the more packets it can buffer. A large buffer space also ensures that all packets can be processed—that is, none will be overwritten before the host can deal with them.

PRODUCTS

Solder-paste inspection system

Agilent Technologies has introduced the Medalist SP50 Series 3 solder-paste inspection system for inspecting printed-circuit-board assemblies. Systems in the Medalist SP50 family offer interchangeable lighting heads and can be deployed at paste or pre- or post-solder as needs change. Links to downstream repair stations and statistical process control tools help users increase yields and improve board quality. *Agilent Technologies, www.agilent.com.*

Vibration isolation workstation

The MK26 Series vibration-control workstation offers excellent vertical and horizontal isolation efficiencies. Adjusted to a ½-Hz natural frequency, the workstation achieves 93% isolation efficiency at 2 Hz, 99% at 5 Hz, and 99.7% at 10 Hz. The workstation has a capacity of 700 lbs and can be used with confocal microscopes, optical microscopes, wafer probers, and atomic-force microscopes. Base price: $6920. *Minus K Technology, www.minusk.com.*

Wafer loaders

Olympus Micro-Imaging has introduced the AL110 Series wafer loaders for thin-wafer inspection. The AL110 can handle 100-mm to 200-mm wafers with thicknesses down to 250 µm. The wafer loaders feature precise centering, and a second back-inspection feature rotates the wafer to provide 100% back macro inspection for improved quality control. *Olympus Micro-Imaging, www.olympusmicroimaging.com.*

GigE CCD camera

The GE680 CCD camera captures 200 frames/s at VGA resolution and up to 1500 frames/s for a 25x25 region-of-interest. It includes a Gigabit Ethernet (GigE) interface and is suitable for a variety of machine-vision applications. The camera is available in monochrome and color models and offers a progressive-scan CCD sensor with global/snapshot shutter, external trigger and sync, general-purpose I/O, and region of interest readout. *Prosilica, www.prosilica.com.*

FireWire-B cameras

The eight models in the FireDragon line of progressive-scan cameras employ FireWire-B (IEEE-1394.b) technology to provide transfer rates of 800 Mbps. Some models deliver full-frame images up to 90 frames/s and resolutions ranging from VGA to UXGA. Both monochrome and color versions are available. Monochrome output can be set for 8 or 10 bits, while color output formats include 24-bit RGB, YUV422, and YUV411. *Toshiba Teli America, www.toshiba-teli.com*


Matrox Imaging Library
Application Development Software

Keithley embraces PXI

Richard A. Quinnell, Contributing Technical Editor, and Martin Rowe, Senior Technical Editor

Instrument maker Keithley has begun a thrust in a new direction for its test instrument line. The company recently adopted PXI as a key element in its latest test system. The Series KPXI is a hybrid system with PXI as the core, augmented with high-performance stand-alone instruments that connect to the core via GPIB and LXI links.

We spoke with Keithley product manager Mark Cejer by phone to discuss the motivation for this new direction at Keithley.

Q: Why did Keithley decide to get into PXI now, nearly 10 years after the introduction of the technology?

A: PXI has started to attain critical mass in our markets. When it was first introduced, PXI tended to target more classic data-acquisition applications of an electrical or mechanical nature. What we are seeing now, however, is that PXI is increasingly being considered by test engineers in the electronics, semiconductor, and wireless industries. So, now our customers are starting to ask for PXI.

INSIDE THIS REPORT

Q: Does this mean that PXI is winning the instrument bus war with LXI?

A: PXI and LXI have to coexist and have to be more complementary as opposed to competitive. No one form factor or communication bus can solve every testing need, and we really ought to utilize the best of each. Let the application determine the right kind of approach. Our intention is to use PXI to complement instruments and help test engineers become more productive. By embracing both LXI and PXI, we can work closely with our customers to help them build more optimum solutions to their electronic test applications.

Q: What makes hybrid systems the right approach?

A: Electronics test system builders need the precision of instrumentation as well as the speed of a well-integrated system. Our hybrid offering can provide that precision as well as dramatically speed test time through parallel processing and concurrent execution.

Q: How does it do that?

A: The PXI controller is the system controller, talking with the LXI and GPIB instruments over their buses. Our SourceMeter instruments with TSP test script processor use the GPIB to download a script that the instrument runs each time it is triggered. The GPIB is used only at initialization. A digital I/O card from the PXI tray triggers the instrument during operation to start it executing its script. The SourceMeter output triggers the RF products, which also have sequencing capability. This distributed operation is the key to the throughput improvement. The bus transfer rate is not the bottleneck in electronics test applications. Things like soak time, switch closures, settling times, and mode changes for the device under test are the holdup. Having distributed processing optimizes triggering, timing, and coordination of the overall system to maximize throughput.

Mark Cejer
Product Manager
Keithley Instruments
Courtesy of Keithley Instruments.

Q: Doesn't this complicate the test-development effort?

A: Yes, but if you try to make things too simple, you end up compromising performance. For our customers, the pressure is intense with respect to profitability, and shaving microseconds off the test time can end up making or breaking their product in the market. They are willing to make the investment to have somewhat more complex programming because the benefits far outweigh the initial cost. □

EDITOR'S NOTE

PXI reaches maturity

Richard A. Quinnell, Technical Editor

It's a bittersweet moment when you realize that your children have grown up. Not too long ago, they needed special care and nurturing. Then, all of a sudden, it seems, their natures have changed and the relationships that once held true need to be re-examined.

Like a growing child, PXI seems to have reached a new level of maturity that merits viewing with new eyes. The adoption of PXI or PCI by Keithley, Agilent, and other companies that have traditionally developed standalone instruments is evidence that PXI and PCI modular instruments have achieved mainstream acceptance. PXI is no longer merely an emerging technology; it is a proven tool for test engineering.

This evidence of maturity by no means suggests that PXI has reached its full potential. As evidence of ongoing progress, witness the debut of the PXI Express specification, which provides for a 45-fold increase in bandwidth over the original PXI. On the applications front, BAE Systems, National Instruments, and Phase Matrix announced last fall that they are collaborating on developing a 26.5-GHz synthetic instrument based on PXI Express—an effort that is expected to yield prototypes this fall.

As the technology continues to grow, we will keep you posted on new design and applications options. We welcome your input about your experiences with PXI and about where you hope the technology is headed. □

Contact Richard A. Quinnell at richquinnell@att.net.

HIGHLIGHTS

Agilent to acquire Acqiris

Agilent Technologies has agreed to acquire Acqiris, a maker of high-speed digitizer cards for the PCI, CompactPCI, and PXI buses. The product line also includes analyzer cards that contain onboard digital signal processors (DSPs) and multichannel instruments made up of the company's cards. The acquisition marks Agilent's first presence in the digitizer card market since the company divested its line of VXI instruments in 2003. It's also the first time in the PXI market in any way for that long-time maker of stand-alone box instruments. www.agilent.com.

Keithley introduces PXI modules

Keithley Instruments, renowned for its bench instruments, recently entered the PXI market with the introduction of a broad line of PXI instrument cards, chassis, controllers, and accessories. The company has introduced eight models of multifunction data-acquisition cards (KPXI-DAQ series), two multifunction cards (KPXI-SDAQ), two analog output cards (KPXI-AO), four digital I/O cards (KPXI-DIO), and a two-channel digitizer (KPXI-AI-2-65M).

The new PXI line also includes two extension interface cards, one of which extends a PXI system by connecting to other PXI chassis. The second interface card lets you control a PXI chassis from a PC through its PCI bus. www.keithley.com.

Webcast overviews PXI digital test

The PXI Systems Alliance and Geotest–Marvin Test Systems have produced a Webcast entitled, "Using PXI Digital Test Instrumentation for Video Test Applications." First aired on December 6, the Webcast is still available on the PXISA Web site.

The Webcast, presented by Dale Johnson, Geotest's customer technical support manager, provides an overview of PXI digital test instrumentation architectures that can be employed for a range of high-performance digital stimulus/response applications including video record/playback. Included is a discussion of how a PXI-based test solution can be used to address a video-test application. www.pxisa.org.

Huntron teams with integrators

Huntron has announced that it has established an authorized integrator program for its TrackerPXI and Access Robotic Probing Station systems. It has signed on Advint (Columbus, OH), Custom Systems Integration (Endicott, NY), and Larson Automation (Fremont, CA). TrackerPXI employs signature-analysis techniques to add component-level diagnostics to existing PXI test platforms. The Access probing stations provide 20-micron accuracy to provide reliable probing of small surface-mount components.

"Huntron traditionally has been involved in stand-alone test solutions; however, our customers are driving us to integrate our TrackerPXI and Access Robotic Probing Station as a complementary diagnostic tool for a wide variety of automatic test equipment. We always try and provide our customers with the most cost-effective solutions, and historically Huntron has very little experience with integration. We thought the best solution for us to support customers was to align our products with industry leaders in the design, development, integration, test, and support of automatic test systems," said Bill Curry, Huntron president. www.huntron.com.

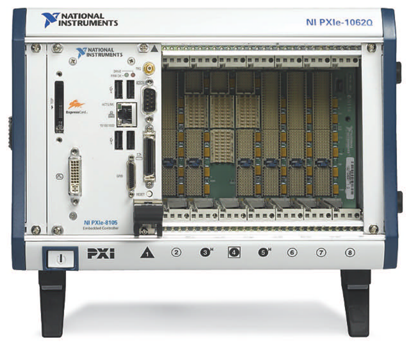
Hybrids jump-start PXI Express

Richard A. Quinnell, Contributing Technical Editor

The PXI Express specification is only a year and a half old, so there are only a few modules available that take advantage of the higher bandwidth it offers. Still, designers should be ready to embrace PXI Express in order to keep their systems upgradable. One key to being prepared is to examine the hybrid PXI/PXI Express backplanes that are now appearing on the market.

PXI Express (PXIe) is an addition to the PXI family of standards and is based on PCI Express. PCI Express replaces the parallel PCI bus with a serial link to achieve higher data rates. The serial link comprises a set of serial "lanes," each of which operates at 2.5 Gbps. The lanes are differential signals that are self-clocking using an 8b/10b coding scheme, which gives each lane a raw data bandwidth of 2 Gbps. Configurations of x1, x2, x4, x8, x12, x16, and x32 lanes are possible, providing a bus bandwidth as much as 45X that of traditional PXI.

Unlike the parallel PCI bus, which must be routed to all its many users,



A hybrid chassis allows designers to mix PXI and PXIe boards, simplifying upgrades as new boards become available. Courtesy of National Instruments.

the serial link is point-to-point. Connections are peer-to-peer and can be made nonblocking. Thus, the bus bandwidth for a PXIe link can be dedicated to the transaction taking place, and simultaneous backplane transfers between two pairs of cards are possible.

In addition to the high-speed data path, PXIe provides enhanced synchronization capabilities. Taking advantage of high-speed differential signaling technology, PXIe distributes a 100-MHz clock to card slots. This both improves the accuracy of timing in the system and reduces the need for clock multipliers to generate frequencies greater than the 10 MHz available on conventional PXI. PXIe also offers differential triggers arranged in a star formation from slot to slot to help enhance timing and synchronization.

Software compatibility with PXI

A key feature of PXIe is that modules based on the standard are fully software compatible with PXI. This compatibility results from hardware within the PXIe interface that automatically handles the serialization of parallel data as well as the out-of-band control signals (such as interrupts), presenting the same interface to application layer software as traditional PXI. The consequence is that operating systems, drivers, and applications code de-

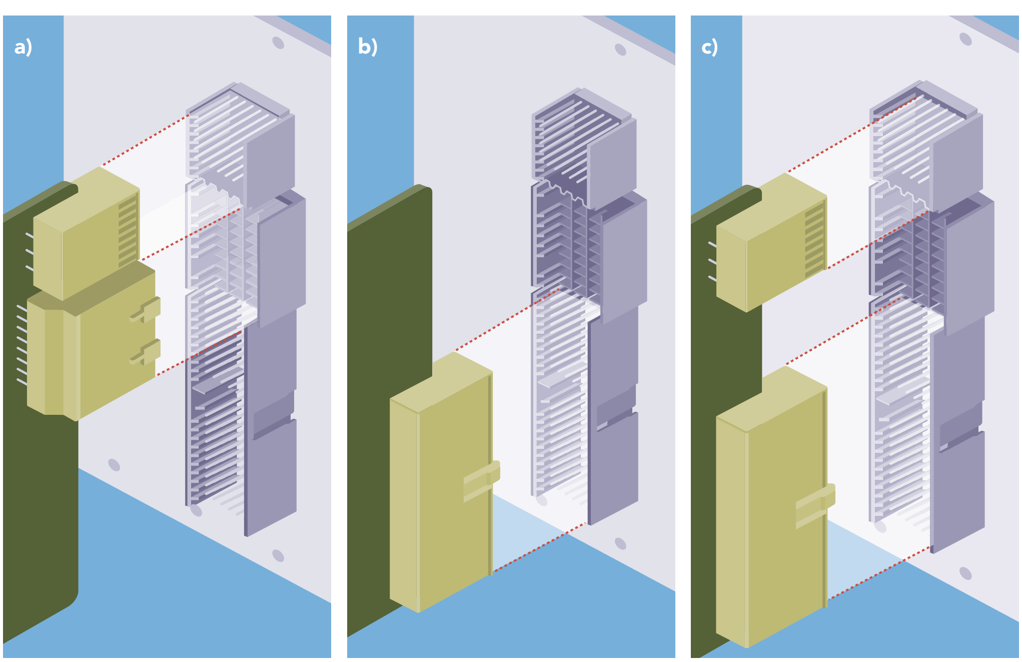


Fig. 1 **The PXIe hybrid chassis has card slots dedicated to a) conventional PXI cards and b) PXIe cards and also includes c) hybrid slots that can accept a CompactPCI card, a PXI card, or a PXIe card.** Courtesy of the PXI Systems Alliance.

veloped for PXI systems can run unaltered on PXIe hardware.

The PXI Systems Alliance (PXISA) released the PXIe specification in August 2005, and as yet only a few compatible products are on the market. These include PXIe controllers from National Instruments, PXIe carrier boards for PMC modules from Radstone Embedded Computing, and a data-recording system from Conduant. The available products are not yet enough to make an entire system based on PXIe. Developers can, however, prepare to capitalize on new PXIe products when they create their next generation of test systems. The trick is to use a hybrid chassis.

Hybrid systems open doors to PXIe

A hybrid PXI/PXIe chassis, such as the eight-slot PXIe-1062 from National Instruments, allows designers to create test systems that use both PXI and PXIe cards. The NI chassis uses a PXIe system controller and a PCI-to-PCIe bridge to support three types of peripheral card slots. One type of slot accepts conventional PXI cards, the second type accepts PXIe cards, and the third type is a hybrid slot (**Figure 1**). The hybrid slot can accept a CompactPCI card, a PXI card, or a PXIe card as long as the card is hybrid-slot compatible. Together, the three slot types give designers considerable flexibility, as they can use various combinations of cards when configuring a system.

Not all PXI cards are hybrid-slot compatible, however, so developers should check their choices carefully. The differences between compatible and noncompatible cards are located in the J2 connector area.

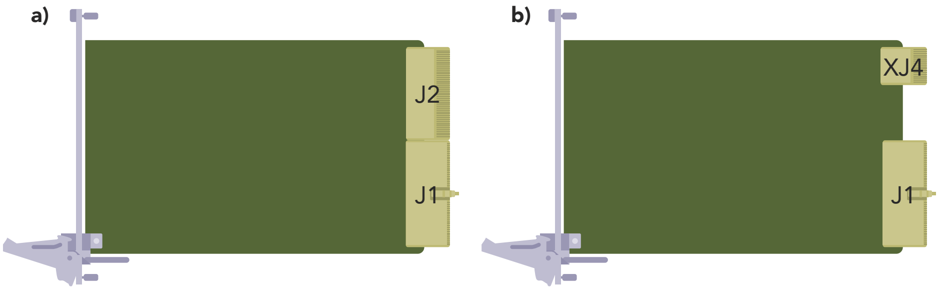


Fig. 2 Legacy PXI cards can be made compatible with the PXIe hybrid slot by replacing the J2 connector with a smaller one.
Courtesy of the PXI Systems Alliance.

The J2 connector carries the PXI local bus as well as power, timing, and synchronization signals. The PXIe card slot replaces the J2 connector of PXI with two connectors: XJ3 and XJ4. The XJ3 connector carries the eight lanes of high-speed PXIe serial signals. The XJ4 connector carries the power, trigger bus, and synchronization signals of PXI.

This arrangement mates with CompactPCI cards that do not use J2, as well as with PXIe cards, which use only XJ3 and XJ4. Conventional PXI cards that use the full J2 connector, however, will not mate with the hybrid socket. To make these cards hybrid-compatible, developers have to depopulate the J2 connector as shown in **Figure 2** and replace it with the XJ4 connector, leaving a space where the XJ3 connector is located.

Many of the new PXI cards coming on the market are now hybrid-slot compatible, so developers will be easily able to create new hybrid systems using new cards. For users that have an inventory of older PXI cards, however, the presence of J2 will prevent their re-use in new hybrid systems. Fortunately, the card manufacturers are starting to offer conversion services. Send them your old board, and for a small fee they will reconfigure it for hybrid-slot compatibility.

Hybrid limitations

Working with a hybrid chassis does have some limitations. One is that the hybrid slot only supports eight lanes, limiting bus bandwidth to 2 Gbytes/s. The second limitation is the elimination of the PXI local bus on the hybrid slots. For many users, these limitations may have no significance. The local bus is seldom used, and a 2-Gbyte/s bandwidth still represents a significant performance boost over conventional PXI. Engineers who do depend on the local bus, however, must be careful to place the cards in the conventional PXI slots only.

The availability of hybrid backplanes helps developers meet both performance and cost goals when designing test systems. Low-bandwidth functions, such as motor control, switching, and general-purpose data acquisition, can remain in the PXI form factor instead of migrating to the higher-performance PXIe bus. This helps keep system costs down, as designers do not need to redesign the modules for low-bandwidth functions in order for the entire system to take advantage of PXIe's higher bandwidth.

At the same time, the hybrid backplane gives high-performance functions, such as high-channel-count data acquisition, high-speed imaging, and direct-conversion RF, an opportunity for performance growth. As PXIe boards for these functions become available, designers can replace the conventional PXI board with the higher-performing board without needing to alter the system software.

By bridging the large legacy world of PXI with the emerging world of PXIe, hybrid chassis offer developers the opportunity to jump start their adoption of the high-performance bus. Eventually, as functions migrate to the new bus, full PXIe system backplanes will emerge. In the meantime, hybrid backplanes are here to smooth the transition. □

PRODUCTS

Signal-capture boards

UK-based DataQuest Solutions has extended its Spectrum M2i range of PCI/PCI-X, CompactPCI, and PXI signal-capture boards to include the 16-bit M2i.46xx series, which feature capture rates up to 3 Msamples/s on up to eight input channels.

The boards capture signals with over 14.5 effective bits for a wide combination of speed and input ranges from ±50 mV to ±10 V. Internal RMS input noise level is in the microvolt region on higher ranges. Each channel uses its own ADC to provide true differential or single-ended input. To enable long capture periods, the boards include 64 Mbytes of storage, which you can expand to 4 Gbytes. Alternatively, you can use the storage as a FIFO buffer for real-time transfers to a PC. The boards operate in PCI or PCI-X slots with 3-V and 5-V I/O voltages. *DataQuest Solutions, www.dqsolutions.co.uk/boardpagead.htm.*

64-bit Windows driver

Strategic Test offers a Windows XP Pro 64-bit driver for its digitizer, arbitrary waveform generator, digital I/O, and digital pattern generator cards. The driver is compatible with all 150 PCI/PCI-X, PXI, and CompactPCI products in the UltraFast family.

Windows XP Pro x64 Edition supports up to 128 Gbytes of RAM and 16 Tbytes of virtual memory, so applications can run faster when handling large data sets.

The Windows XP Pro x64 driver is supplied at no cost and can be downloaded by existing customers from the company's Web site. The same programming concept found in the other Windows and Linux drivers has been employed, allowing you to upgrade your operating system without modifying your application code. *Strategic Test, www.strategic-test.com.*

PXI platform suites

Aeroflex announced that it has added new wireless test capabilities to its PXI 3000 Series modular wireless test platform to aid the rapid production testing of the most popular consumer mobile devices.

Within a single software-definable PXI modular platform, the Aeroflex PXI 3000 Series now includes support for WiMax OFDMA, 1xEvDO, and HSUPA. With the addition of these new measurement suites, the Aeroflex modular RF test systems now allow testing of cellular, WLAN, and WiMax in one product. *Aeroflex, www.aeroflex.com.*

PRODUCTUPDATE

High-voltage power-bus converter

Vicor's high-voltage V•I Chip Bus Converter offers a power density of greater than 1000 W/in^3. Designated B352F110T30, the converter employs the company's Sine Amplitude Converter (SAC) technology and provides better than 95% efficiency. It operates from a 330- to 365-VDC primary bus to deliver an isolated 10.3- to 11.4-V secondary.

The converter can be used individually, or multiple converters can be used in parallel for higher power. In addition, outputs may be connected in series to create higher voltages for applications such as RF amplifiers. The module package measures 1.28x0.87x0.26 in. and is compatible with standard pick-and-place surface-mount machinery and assembly processes. It offers low junction-to-case and junction-to-board thermal resistance to facilitate thermal management and reduce the need for heat sinks.

Base price: $37.40 in OEM quantities. *Vicor, www.vicorpower.com.*

Agilent announces four Genesys EDA suites

Agilent Technologies has announced four new Genesys EDA software configurations priced under $10,000. The new packages support linear, nonlinear, and electromagnetic RF system simulation and RF synthesis.

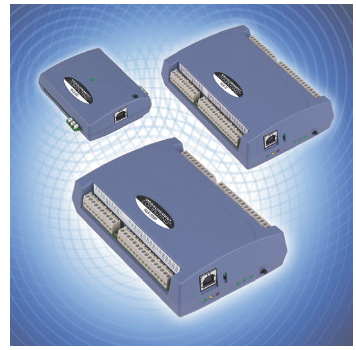
Configurations for the new suites include:

- Genesys Core, which provides the schematic environment as well as layout, linear simulation, optimization, Monte Carlo analysis, and data post-processing;
- Genesys Designer Pro, which adds eight passive and active circuit-synthesis modules for RF circuit design;
- Genesys Nonlinear Pro, which adds harmonic balance and planar EM simulation to Genesys Core to enable true nonlinear transceiver design; and
- Genesys Comms Pro, which adds the Spectrasys and WhatIF RF architecture tools to Genesys Core to allow high-performance RF system design.

Agilent also announced a fifth new suite, Genesys Integrated, which combines all the Genesys environment and simulation modules into one software platform.

Base price: $3995, including 12 months of software maintenance plus an upgrade to the next Genesys release, planned for March. *Agilent Technologies, www.agilent.com/find/eesof.*

Temperature measurements go wireless



Measurement Computing has introduced IEEE 802.15.4 wireless capabilities to its USB-based temperature monitors. The new WLS-TC and WLS-TEMP modules are based on the company's USB-TC and USB-TEMP devices but add an RF module that permits wireless data transfer. The WLS-TC input module accepts eight channels of type J, K, R, S, T, N, E, and B thermocouples. The WLS-TEMP module accepts the same thermocouples and also supports RTD, thermistor, and semiconductor temperature sensors.

Both models are capable of 150-ft range indoors and 2460-ft range outdoors in direct-line-of-sight applications. To use the wireless capability, you need the WLS-IFC interface module, which connects to a PC's USB port and provides access to an unlimited number of WLS-TC and WLS-TEMP devices.

Prices: WLS-TC—$549 ($599 with WLS-IFC); WLS-TEMP—$749 ($799 with WLS-IFC); additional WLS-IFC wireless interfaces—$149. *Measurement Computing. www.measurementcomputing.com.*

Embedded controller has multiple I/Os

Adlink's GEME-5000 embedded controller offers two serial ports as well as USB, IEEE 1394, parallel, Ethernet, and Compact Flash ports. All I/O ports, including keyboard/mouse and VGA, are accessible from the front-panel.

You can power the controller from an AC mains cord or from DC, making it useful for remote applications such as automotive testing. The GEME-5000, running a Pentium processor up to 1.4 GHz, comes with 256 Mbytes of RAM and runs Windows 2000/XP, Embedded XP, WinCE. Net, or Linux.

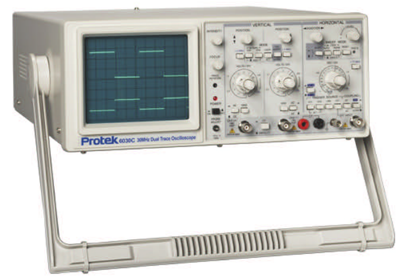
Base price: $2150. *Adlink Technology, www.adlinktech.com.*

> > > > > > >

Dual-trace oscilloscopes

Equipped with a high-brightness CRT, the Model 6030C dual-trace analog oscilloscope from Protek comes with a pushbutton-activated component tester for checking inductors, capacitors, and diodes via a characteristics waveform displayed on the screen. The scope provides a 30-MHz vertical bandwidth (–3 dB) and an alternate trigger function for stable display of unrelated signals. It also features 5X magnification for vertical input and 10X magnification for horizontal sweep. A TV synch filter is standard.

A second dual-trace analog scope, the 20-MHz Model 6020, provides alternate magnification for the simultaneous display of the main and 10X magnified waveforms. This low-power (40 W) unit



also furnishes alternate trigger and auto trigger functions for display stability, z-axis modulation, and 10X magnification for horizontal sweep.

Base prices: Model 6030C—$484; Model 6020—$449. *Protek Test & Measurement, www.protektest.com.*

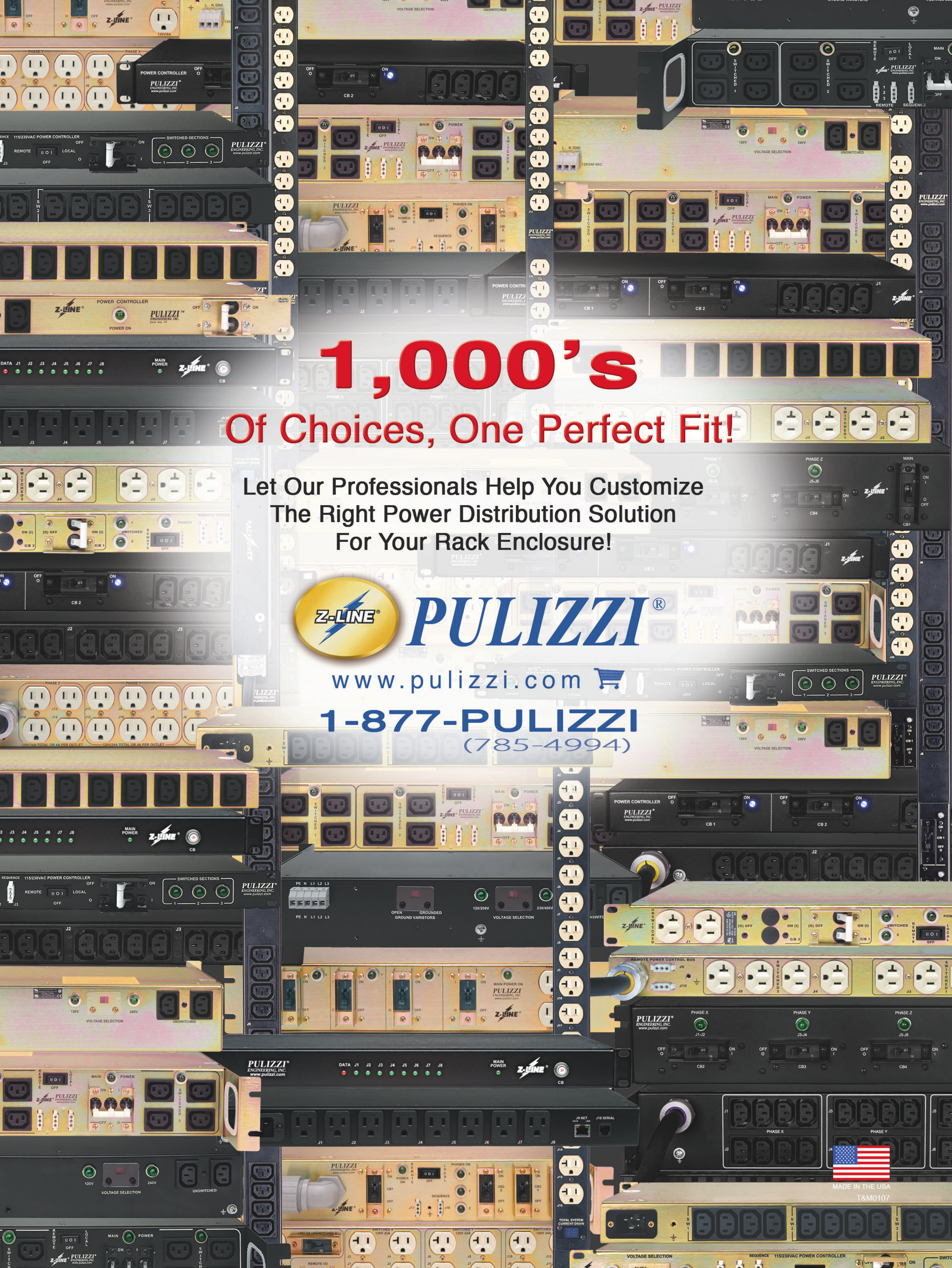
PCI Express exerciser

A companion development tool for LeCroy's PETracer Summit protocol analyzer, the LinkUP Trainer helps you qualify PCI Express products through Link Training and Status State Machine (LTSSM) testing. The card-based exerciser, which operates at both PCI Express Gen1 and Gen 2 speeds, enables you to find issues that can affect interoperability.

LinkUP generates training sequences at 2.5 Gbps (Gen 1) and 5 Gbps (Gen 2) for lane widths ranging from x1 to x16. It can be configured to transition to various states and to change data rates in order to test speed negotiation. You can also change each PCI Express lane's parameters, such as lane skew, polarity, and scrambling, to expose physical layer issues.

The user interface runs on a separate host PC connected to the LinkUP system via either a USB cable or Ethernet 10/100-Mbps port. System status updates automatically at specified intervals. Status reports include current operating width, data rate, link number, lane reversal status, RX polarity, scrambling status, and advertised parameters of the device under test.

LeCroy, www.lecroy.com.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400-W/600-W modular power supplies

The Xhite series of modular power supplies from Excelsys offers full load operation up to 70°C, making the supplies suitable for operation in harsh environments that have high ambient temperatures and wide temperature fluctuations. The series comprises two PowerPac chassis, with ratings of 400 W or 600 W, and a complete family of field-configurable plug-in DC output modules. The PowerPacs accept universal input from 85 VAC to 264 VAC with plug-in modules offering single and dual outputs ranging from 1.5 VDC to 58 VDC. All configurations are RoHS-compliant, approved to UL60950/EN60950 safety standards, and are rated for EN55022/FCC Level B conducted and radiated emissions.

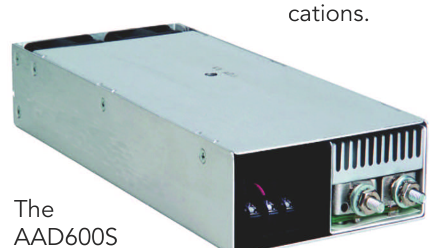
Xhite power supplies employ a two-transistor forward-converter front end and zero-voltage resonant switching with plug-in DC output modules that use planar magnetics, surface-mount components, and high-efficiency DC/DC conversion techniques. The supplies are packaged in a compact 9.85x5.00x1.57-in. form factor.

DC outputs are floating with no minimum load requirements, ±0.1% line regulation, and ±0.2% load regulation. Outputs can be connected in series or parallel for increased power, and they feature comprehensive protection against over-voltage, over-current, and over-temperature conditions. Standard signal options include mains power fail, global inhibit/enable, 5-V standby, output power good, output inhibit/enable, remote sense, and remote adjust.

Excelsys Technologies, www.excelsys.com.

Switching power supplies

Tamura's AAD600S series of single-output switching power supplies offers 600 W of tightly regulated power in a compact package that is only 9.00x4.00x1.59 in., making it useful for low-profile, 1U-high applications.



The AAD600S provides a single output of 12 VDC, 15 VDC, 24 VDC, 28 VDC, 36 VDC, or 48 VDC and accommodates a universal AC input range of 85 VAC to 264 VAC, 47 Hz to 63 Hz.

The unit also provides active power factor correction for EN61000-3-2 Class D compliance. Built-in cooling fans and over-current, over-temperature, and over-voltage protection circuits ensure reliable performance for industrial, datacom, networking, and telecom

applications. Status and control functions include remote sense, DC OK, power fail, remote on/off, and single-wire current share.

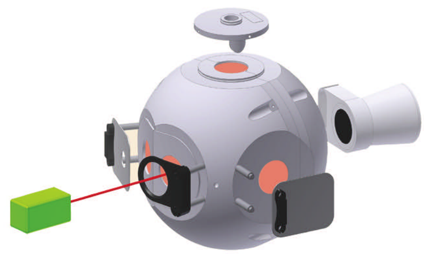
Options include inverted status/control signals, internal OR-ing diodes, and auto-recovery, hiccup, latch-off, and fold-back protection modes. All models are RoHS-compliant, bear the CE Mark (LVD), and are rated for EN55022 (Level B) and FCC Part 15 Class B emissions.

Tamura, www.tamuracorp.com.

Integrating sphere

Gigahertz-Optik's UPB-150-ART integrating sphere is designed for multipurpose single- or double-beam reflectance and transmittance measurements in both ±8° and 0° geometries. The five precision CNC-machined application ports offer a symmetrical knife-edge design to guarantee optimum light input.

The sphere is coated with ODP97, a white diffuse paint that exhibits a typical reflectance of 97% in the visible spectral range with a usable range specified from 300 nm to 2400 nm. Standardized port interfaces allow simple mounting of Gigahertz-Optik detector heads, fiber-optic adapters, light sources, light traps, and other accessories.



You can use the UPB-150-ART sphere to perform standard reflection and transmission measurements in accordance with the DIN-5036, CIE 128, and ISO 13468 specifications.

Gigahertz-Optik, www.gigahertz-optik.com.

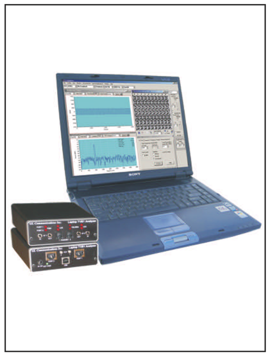
Network analyzer software

Rohde & Schwarz has expanded its high-end R&S ZVA network analyzer with the addition of the R&S ZVA-K7 software option for pulse-profile measurements on semiconductors and antenna systems. The software option can derive and display absolute levels or S-parameters in real time on pulses down to 50 ns with a measurement resolution of 12.5 ns.

The ZVA-K7 software option operates with periodic or single pulses. You can generate pulsed RF signals by modulating the analyzer's internal generator with an external pulse generator or by using a completely separate signal source such as an R&S SMR. You can set measurement bandwidth to 30-MHz maximum, which allows rise times of 33 ns. Pre- and post-trigger settings enable you to position the measurement window relative to the pulse signal and selectively measure pulse intervals.

Rohde & Schwarz, www.rohde-schwarz.com.

USB BASED PORTABLE T1/E1 ANALYZER



New USB based T1/E1 Analyzer is the world's most powerful and complete voiceband, protocol, and BERT analyzer. Analysis and emulation of all signal types including voice, digits, tones, fax, modem and all protocols - HDLC, ISDN, SS7, CAS, GSM, GPRS, CDMA. Capable of T1 /E1 visualization, capture, storage, analysis, emulation, and convenient features like portability, remotability, and scripting.

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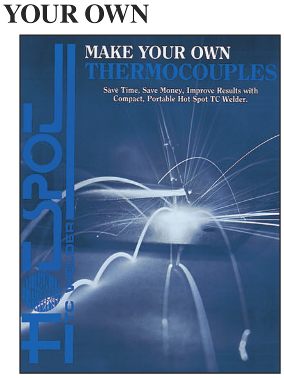

The HOTSPOT welding unit allows thermocouple wire to be formed into freestanding head or butt welded junctions, or to be directly welded to metal surfaces. The HOTSPOT provides a quick, simple, accurate, low cost means of fabricating thermocouples on a "when needed, where needed" basis. Brochure and specification sheet available.

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MICHAEL VOHRER
President and CEO
Rohde & Schwarz
Munich, Germany

Michael Vohrer studied communications engineering and began his professional career at Rohde & Schwarz in 1975. Starting as a development engineer, he rose to become head of the Test and Measurement Division in 1996, responsible for the marketing, design, and development of T&M instruments and systems. In 2003, Vohrer became a member of the Executive Board and was appointed president and COO, in charge of the Broadcasting Division and the Test and Measurement, Radiomonitoring and Radiolocation Division. In January 2006, he became CEO of the company, which employs 6800 people in more than 70 countries.

Contributing editor Larry Maloney spoke with Vohrer about industry trends in a recent telephone interview.

Imagining tomorrow's products today

Q: How do you assess the progress of your company after a year as CEO?

A: We continue to build on the Rohde & Schwarz reputation for quality products and fast customer service. In the 2005–2006 fiscal year, which ended in June, we had net revenues of approximately €1.3 billion (approximately $2.52 billion), about an 18% increase over the 2004–2005 year.

Q: What do you see as the biggest challenges in continuing this growth?

A: The Internet is turning the world into a village. Our customers, especially the large mobile-communications companies, are becoming more international. So, we need to offer a global line-up of products, as well as the same excellent service, no matter where our customers are located. We also must be sensitive to the different mindsets and cultures of employees and customers worldwide. And we need to put continued emphasis on innovation in products, sales, and service.

Q: What were your most significant product introductions of 2006?

A: A major new product for EMC test is our R&S ESU family of EMI test receivers. These receivers use FFT-based test methods that perform measurements up to 100 times faster than earlier receivers. Another notable product is the R&S FSUP, which combines in one instrument a sophisticated spectrum analyzer and a phase-noise tester. The result is a much simpler and less costly test set for engineers who develop communications, broadcast, and radar systems.

For mobile digital TV, we developed a new test platform, the SFU, which is compatible with all five global standards: DVB-H, T-DMB, ISDB-T, DMB-TH, and MediaFlo in the US. We believe we have an advantage in this market because of our long experience with test platforms for producers of mobile phones. Increasingly, mobile-phone technology will be combined with mobile digital TV standards.

Q: How about new technologies?

A: Standards in such fields as mobile communications are expanding continually. So, our company needs to be integrally involved in defining tomorrow's standards. That means working closely with standards groups and large customer companies all over the world. We plan to offer test and measurement solutions at a very early stage for emerging generations of mobile-phone and mobile-radio applications. For instance, we are up-to-date on a large product portfolio for HSPA (high-speed packet access), a technology that will allow mobile phones to provide data rates similar to wireless LAN and WiMax.

At the 2006 Electronica show, we demonstrated the first solutions for generating and analyzing signals for UMTS Long Term Evolution (LTE), a technology that allows high-data-rate applications for future mobile phones. WiMax also is very important, and we provide a wide range of RF test devices for development and production.

Q: What other steps do you take to foster innovation?

A: As a private company, we have greater freedom to pursue technologies that customers are going to need two, three, or five years from now. Late in 2005, we opened in Munich a new 16,000-m^2 R&D facility, which is home to about 500 development engineers. There, we follow a strategy of keeping in our own hands technologies that are core to our competitive advantage, such as microwave innovations, very fast analog-to-digital converters, and integration of functionality on ICs. If I can use only those technologies that I can buy, then I am limited to doing what others do. That is not enough for Rohde & Schwarz. T&MW

Michael Vohrer offers additional comments on LXI, telecommunications issues, and new growth opportunities in the online version of this interview: www.tmworld.com/2007_02.